

- 1) K. Shibahara, S. Nishino, and H. Matsunami, “*Metal-oxide-semiconductor characteristics of chemical vapor-deposited cubic-SiC*”, Jpn. J. Appl. Phys., **23** (1984) L862-L864.
- 2) S. Dohmae, K. Shibahara, S. Nishino, and H. Matsunami, “*Plasma-etching of CVD grown cubic SiC single crystals*”, Jpn. J. Appl. Phys., **24** (1985) L873-L875.
- 3) K. Shibahara, T. Saito, S. Nishino, and H. Matsunami, “*Fabrication of inversion-type n-channel MOSFETs using cubic SiC on Si(100)*”, IEEE Electron Device Lett., **7** (1986) 692-693.
- 4) K. Shibahara, S. Nishino, and H. Matsunami, “*Surface-morphology of cubic SiC(100) grown on Si(100) by chemical vapor deposition*”, J. Crystal Growth **78** (1986) 538-544.
- 5) K. Shibahara, S. Nishino, and H. Matsunami, “*Antiphase-domain-free growth of cubic SiC on Si(100)*”, Appl. Phys. Lett., **50** (1987) 1888-1890.
- 6) K. Shibahara, N. Kuroda, S. Nishino, and H. Matsunami, “*Fabrication of p-n-junction diodes using homoepitaxially grown 6H-SiC at low temperature by chemical vapor-deposition*”, Jpn. J. Appl. Phys., **26** (1987) L1815-L1817.
- 7) K. Shibahara, T. Takeuchi, T. Saitoh, S. Nishino and H. Matsunami, “*Inversion-type MOS field effect transistors using CVD grown cubic SiC on Si*”, Proc. Mat. Res. Soc., **97** (1987) 247-252.
- 8) M. Iwami, M. Kusaka, M. Hirai, H. Nakamura, K. Shibahara, and H. Matsunami, “*A New application of soft-X-ray spectroscopy to a non-destructive analysis of a film substrate contact system - Carbonized-layer (ultra-thin-film) Si(100)*”, Surf. Sci., **199** (1988) 467-475.
- 9) M. Iwami, M. Kusaka, M. Hirai, H. Nakamura, T. Koshikawa, K. Shibahara, and H. Matsunami, “*Compositional analysis of semiconductor heterojunctions - Structure of SiC (thin buffer layer)/Si(100) system*”, Nucl. Instr. and Meth. B, **33** (1988) 615-618.
- 10) K. Shibahara, T. Takeuchi, S. Nishino, and H. Matsunami, “*Electrical-properties of undoped and ion-implanted cubic SiC grown on Si(100) by chemical vapor-deposition*”, Jpn. J. Appl.

Phys., 28 (1989) 1341-1347.

- 11) H. Hida, Y. Tsukada, Y. Ogawa, H. Toyoshima, M. Fujii, K. Shibahara, M. Kohno, and T. Nozaki, “*High-speed and large noise margin tolerance E/D logic gates with LDD structure DMTs fabricated using selective RIE technology*”, IEEE Trans. Electron Devices, **36** (1989) 2223-2230.
- 12) K. Shibahara, Y. Ogawa, H. Toyoshima, H. Hida, T. Maeda, and K. Ohata, “*Low-temperature buffer introduction into self-aligned refractory-metal gate DMTs*”, IOP Conf. Ser., **112** (1990) 257-262.
- 13) A. Tanabe, T. Takeshima, H. Koike, Y. Aimoto, M. Takeda, T. Ishijima, N. Kasai, H. Hada, K. Shibahara, T. Kunio, T. Tanigawa, T. Saeki, M. Sakao, H. Miyamoto, H. Nozue, S. Ohya, T. Murotani, K. Koyama, and T. Okuda, “*A 30-ns 64-Mb DRAM with built-in self-test and self-repair function*”, IEEE J. Solid-State Circuits, **27** (1992) 1525-1533.
- 14) T. Sugibayashi, T. Takeshima, I. Naritake, T. Matano, H. Takeda, Y. Aimoto, K. Furuta, M. Fujita, T. Saeki, H. Sugawara, T. Murotani, N. Kasai, K. Shibahara, K. Nakajima, H. Hada, T. Hamada, N. Aizaki, T. Kunio, E. Kakehashi, K. Masumori, and T. Tanigawa, “*A 30-ns 256-Mb DRAM with a multidivided array structure*”, IEEE J. Solid-State Circuits, **28** (1993) 1092-1098.
- 15) T. Sugibayashi, I. Naritake, S. Utsugi, K. Shibahara, R. Oikawa, H. Mori, S. Iwao, T. Murotani, K. Koyama, S. Fukuzawa, T. Itani, K. Kasama, T. Okuda, S. Ohya, and M. Ogawa, “*A 1-Gb DRAM for file applications*”, IEEE J. Solid-State Circuits, **30** (1995) 1277-1280.
- 16) T. Doi, T. Namba, A. Uehara, M. Nagata, S. Miyazaki, K. Shibahara, S. Yokoyama, A. Iwata, T. Ae, and M. Hirose, “*Optically interconnected Kohonen net for pattern recognition*”, Jpn. J. Appl. Phys., **35** (1996) 1405-1409.
- 17) T. Namba, A. Uehara, T. Doi, T. Nagata, Y. Kuroda, S. Miyazaki, K. Shibahara, S. Yokoyama, A. Iwata, and M. Hirose, “*High-efficiency micromirrors and branched optical waveguides on Si chips*”, Jpn. J. Appl. Phys., **35** (1996) 941-945.

- 18) H. Goto, K. Shibahara, and S. Yokoyama, “*Atomic layer controlled deposition of silicon nitride with self-limiting mechanism*”, Appl. Phys. Lett., **68** (1996) 3257-3259.
- 19) K. Shibahara, N. Mifudi, K. Kawabata, T. Kugimiya, H. Furumoto, M. Tauno, S. Yokoyama, M. Nagata, S. Miyazaki, and M. Hirose, “*Low Resistive Ultra Shallow Junction for Sub 0.1mm MOSFETs Formed by Sb Implantation*”, International Electron Devices Meeting (IEDM) , San Francisco 1996., pp.579 - 582.
- 20) S. Yokoyama, H. Goto, T. Miyamoto, N. Ikeda, and K. Shibahara, “*Atomic layer controlled deposition of silicon nitride and in situ growth observation by infrared reflection absorption spectroscopy*”, Appl. Surf. Sci., **112** (1997) 75-81.
- 21) J. Maeda, Y. Sasaki, N. Dietz, K. Shibahara, S. Yokoyama, S. Miyazaki, and M. Hirose, “*High-rate GaAs epitaxial lift-off technique for optoelectronic integrated circuits*”, Jpn. J. Appl. Phys., **36** (1997) 1554-1557.
- 22) H. Tobimatsu, Y. Inoue, T. Seto, K. Okuyama, T. Fujii, K. Shibahara, S. Yokoyama, and M. Hirose, “*Reduction of gaseous contamination by UV/photoelectron method*”, IEEE Trans. Semiconductor Manufacturing, **11** (1998) 9-12.
- 23) K. Shibahara, H. Furumoto, K. Egusa, M. Koh and S. Yokoyama, “*Dopant loss origins of low energy implanted arsenic and antimony for ultra shallow junction formation*”, Mat. Res. Soc. Symp. Proc., **532** (1998), pp. 23-28.
- 24) K. Egusa and K. Shibahara, “*Influence of high dose low energy ion implantation on dopant depth profile*”, Abst. of Int. Conf. on Ion Implantation Tech. (IIT'98), pp. P1-145.
- 25) M. Koh, K. Egusa, H. Furumoto, K. Shibahara, S. Yokoyama and M. Hirose, “*Quantitative evaluation of dopant loss in low energy As implantation for low-resistive, ultra shallow source/drain formation*”, Extend. Abst. of the Int. Conf. on Solid State Devices and Materials (SSDM'98), pp. 18-19.

- 26) M. Tsuno, S. Yokoyama, and K. Shibahara, “*Study of electrical characteristics improvements in sub-0.1 μm gate length MOSFETs by low temperature operation*”, IEICE Trans. Electron. **E81-C** (1998), 1913-1917.
- 27) M. Tsuno, S. Yokoyama and K. Shibahara, “*New Ar-plasma cleaning process for reduction of Al/TiSi₂ contact resistance*”, Jpn. J. Appl. Phys., **37** (1998) 5902-5905.
- 28) M. Koh, K. Iwamoto, W. Mizubayashi, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Yokoyama, S. Miyazaki, M. Miura, and M. Hirose, “*Threshold voltage fluctuation induced by direct tunnel leakage current through 1.2-2.8 nm thick gate oxides for scaled MOSFETs*”, International Electron Devices Meeting (IEDM), San Francisco, 1998 pp.919-922.
- 29) M. Koh, K. Egusa, H. Furumoto, T. Shirakata, E. Seo, K. Shibahara, S. Yokoyama, and M. Hirose, “*Quantitative evaluation of dopant loss in 5-10 keV As ion implantation for low-resistive, ultrashallow source/drain formation*”, Jpn. J. Appl. Phys., **38** (1999) 2324-2328.
- 30) M. Tsuno, M. Tanaka, M. Koh, K. Iwamoto, H. Murakami, K. Shibahara, and M. Mattausch, “*Suppression of reverse-short-channel effect in sub-0.1 μm n-MOSFETs with Sb S/D implantation*”, Electron. Lett., **35** (1999) 508-509.
- 31) Y. Sasaki, T. Katayama, T. Koishi, K. Shibahara, S. Yokoyama, S. Miyazaki, and M. Hirose, “*High-speed GaAs epitaxial lift-off and bonding with high alignment accuracy using a sapphire plate*”, J. Electrochem. Soc., **146** (1999) 710-712.
- 32) Y. Aoki, K. Shibahara, S. Yokoyama, and N. Kawakami, “*Evaluation of stress induced defects due to recessed LOCOS process*”, J. Korean Phys. Soc. **35**. Suppl. (1999), pp. S76-S79.
- 33) T. Hatano, A. Nomura, M. Yoshida, A. Nakajima, K. Shibahara and S. Yokoyama, “*Calculation of electrical properties of novel double-barrier metal oxide semiconductor transistors*”, Jpn. J. Appl. Phys., **38** (1999) 399-402.

- 34) K. Shibahara, K. Egusa, and K. Kamesaki, “*Improvement in sheet resistance of Sb-doped ultra shallow junction by dopant pileup reduction at the SiO₂/Si interface*”, Extend. Abst. of the Int. Conf. on Solid State Devices and Materials (SSDM'99), pp. 514-515.
- 35) K. Shibahara, K. Egusa, K. Kamesaki, and H. Furumoto, “*Improvement in antimony-doped ultra shallow junction sheet resistance by dopant pileup reduction at the SiO₂ /Si interface*”, Jpn. J. Appl. Phys., **39** (2000) 2194-2197.
- 36) K. Shibahara and D. Onimatsu “*Antimony clustering due to high-dose implantation*”, MRS 2000 Spring(San Francisco), MRS Online Proceedings Library / Volume 610 / B8.5
- 37) S. Nakamura, M. Itano, H. Aoyama, K. Shibahara, S. Yokoyama, and M. Hirose, “*Comparative studies of PFC alternative gas plasmas for contact hole etch*”, Proc. of 22th Symp. on Dry Process (2000) pp. 199-204.
- 38) M. Hirose, M. Koh, W. Mizubayashi, H. Murakami, K. Shibahara, and S. Miyazaki, “*Fundamental limit of gate oxide thickness scaling in advanced MOSFETs*”, Semiconductor Sci. & Technol. **15** (2000) 485-490.
- 39) M. Hirose, W. Mizubayashi, Khairurrijal, M. Ikeda, H. Murakami, A. Kohno, K. Shibahara, and S. Miyazaki, “*Ultrathin gate dielectrics for silicon nanodevices*”, Supperlattices & Microstructures, **27** (2000) 383-393.
- 40) M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, and M. Hirose, “*Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current*”, IEEE Trans. Electron Dev., **48** (2001) 259-264.
- 41) K. Shibahara, “*Doping issues for sub-100 nm MOSFETs*”, Proc. of 2001 Korea-Japan Joint Workshop on Advanced Semiconductor Processes and Equipments (APSE2001), pp. 160-164, 2001.

- 42) D. Onimatsu and K. Shibahara, “*Influence of extension formation process of indium halo profile*”, Extend. Abst. of the Int. Conf. on Solid State Devices and Materials (SSDM2001), pp. 184-185, 2001
- 43) K. Shibahara, Y. Ishikawa, D. Onimatsu, N. Maeda, A. Mineji, K. Kagawa, A. Matuno, and T. Nire, “*Antimony behavior in laser annealing process for ultra shallow junction formation*”, Extend. Abst. of the Int. Conf. on Solid State Devices and Materials (SSDM2001), pp. 236-237, 2001
- 44) K. Shibahara, T. Oda, and T. Kikkawa, “*Copper drift in low dielectric constant insulator films caused by O_2^+ primary ion beam*”, Abst. 13th Int. Conf. on Secondary Ion Mass Spectrometry and Related Topics (SIMSXIII), p. 37, 2001.
- 45) D. Notsu, N. Ikeuchi, Y. Aoki, N. Kawakami, and K. Shibahara, “*Fabrication of 100 nm width fine active-region using LOCOS isolation*”, IEICE Trans. Electronics, **E85-C** (2002) 1119-1123
- 46) T. Amada, N. Maeda, and K. Shibahara, “*Degradation in a molybdenum-gate MOS structure caused by N^+ ion implantation for work function control*”, Mat. Res. Soc. Symp. Proc. **716** (2002) 299-314.
- 47) K. Shibahara, “*Ultra-shallow junction formation with antimony implantation*”, IEICE Trans. Electron., **E.85-C** (2002) 1091-1097 (**Invited**).
- 48) D. Notsu, N. Ikechi, Y. Aoki, N. Kawakami, and K. Shibahara, “*Fabrication of 100 nm width fine active-region using LOCOS isolation*”, IEICE Trans. Electron., **E.85-C** (2002) 1119-1123.
- 49) K. Shibahara, D. Onimatsu, Y. Ishikawa, T. Oda, and T. Kikkawa, “*Copper drift in low dielectric constant insulator films caused by O_2^+ primary ion beam*”, Appl. Surf. Sci., **203-204** (2002) 387-390.

- 50) A. Matsuno, K. Kagawa, Y. Niwatsukino, T. Nire, and K. Shibahara, “*Pulse duration effects on laser anneal shallow junction*”, Proc. of the 2nd Int. Semiconductor Tech. Conf. (ISTC2002), Vol.2002-17, pp. 148-156, 2002.
- 51) N. Maeda, D. Onimatsu, Y. Ishikawa and K. Shibahara, “*Gate-extension overlap control by Sb tilt implantation*”, Proc. of the 2nd Int. Semiconductor Tech. Conf. (ISTC2002), Vol.2002-17, pp. 165-171, 2002.
- 52) K. Kagawa, Y. Niwatsukino, M. Matsuno, and K. Shibahara, “*Influence of pulse duration on KrF excimer laser annealing process for ultra shallow junction formation*”, Int. Workshop on Junction Tech. (IWJT'02), pp. 31-34, 2002.
- 53) K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno, and K. Shibahara, “*Formation of low-resistive ultra-shallow n⁺/p junction by heat-assisted excimer laser annealing*”, Int. Workshop on Junction Tech. (IWJT'02), pp. 35-36, 2002.
- 54) K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno, and K. Shibahara, “*Defect density reduction and sheet resistance improvement by multi-pulse KrF-excimer-laser annealing*”, Extend. Abst. Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors (USJ 2003), pp. 98-103, 2003.
- 55) K. Imai, S. Maruyama, T. Suzuki, T. Kudo, S. Miyake, M. Ikeda, T. Abe, S. Masuda, A. Tanabe, J.-W. Lee, K. Shibahara, S. Yokoyama and H. Ooka, “*60-nm gate length SOI CMOS technology optimized for system-on-a-SOI-chip solution*”, Proc. of the 203rd Meeting of Electrochemical Society, Silicon-on-insulator Technology and Devices XI, pp. 149-158, (2003).
- 56) K. Imai, S. Shishiguchi, K. Shibahara and S. Yokoyama, “*Phosphorus-assisted low-energy arsenic implantation technology for n-channel metal-oxide-semiconductor field-effect transistor source/drain formation process*”, Jpn. J. Appl. Phys., **42** (2003) 2654-2659.

- 57) M. Hino, T. Amada, N. Maeda, and K. Shibahara, “*Influence of nitrogen profile on metal workfunction in Mo/SiO₂/Si MOS structure*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 494-495, 2003.
- 58) M. Murakawa, K. Shibahara, Y. Oda, T. Higuchi, and K. Nishi, “*Ultra-shallow boron profile fitting compensating for surface contamination by utilizing genetic algorithms*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 504-505, 2003.
- 59) K. Shibahara, K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, and A. Matsuno, “*KrF excimer laser annealing for ultra shallow junction formation: approach for irradiation energy density reduction*”, Extend. Abst. 11th Int. Conf. on Adv. Thermal Processing of Semiconductors (RTP 2003), pp. 13-16, 2003 (**Invited**).
- 60) S. Nakamura, M. Itano, H. Aoyama, K. Shibahara, S. Yokoyama and M. Hirose, “*Comparative studies of perfluorocarbon alternative gas plasmas for contact hole etch*”, Jpn. J. Appl. Phys., **42** (2003) 5759-5764.
- 61) Q. Khosru, S. Yokoyama, A. Nakajima, K. Shibahara, T. Kikkawa, H. Sunami, and T. Yoshino, “*Organic contamination dependence of process-induced interface trap generation in ultrathin oxide metal oxide semiconductor transistors*”, Jpn. J. Appl. Phys., **42** (2003) L1429-L1432.
- 62) M. Shibahara, S. Kotake, T. Inoue, A. Matsuno, K. Kagawa and K. Shibahara, “*Molecular dynamics simulation on excimer laser annealing process for ultra shallow junction formation*”, The 1st Int. Symp. on Micro & Nano Technology, pp. VIII-1-02-1-VIII-1-02-5, 2004.
- 63) T. Eto, and K. Shibahara, “*Precise depth profiling of sub-keV implanted arsenic*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'04), pp. 532-533, 2004.
- 64) K. Sano, M. Hino, N. Ooishi, and K. Shibahara, “*Workfunction tuning using various impurities for fully silicided NiSi gate*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'04), pp. 456-457, 2004.

- 65) E. Takii, T. Eto, K. Kurobe, A. Matsuno, and K. Shibahara, “*Merits and demerits of light absorber for ultra shallow junction formation by green laser annealing*”, Int. Conf. on Ion Implantation Technology (IIT'04), p. 63, 2004.
- 66) K. Shibahara, K. Kurobe and T. Eto, “*Sub-20-nm junction formation by heat-assisted laser annealing*”, Proceedings of 2004 Korea-Japan Joint Workshop on Advanced Semiconductor Processes and Equipments (ASPE 2004), pp. 162-165.
- 67) T. Hosoi, M. Hino, K. Sano, N. Ooishi, and K. Shibahara, “*Molybdenum-gate MOSFET threshold voltage modification based on two-dimensional nitrogen distribution control in gate electrode*”, Abstracts of MRS 2005 spring meeting, pp.191-192. (Oral presentation G14.5, Proceedings for the symposium G was not published.)
- 68) K. Shibahara, K. Kurobe, T. Eto, and Y. Ishikawa, “*Diffusion-less junction formation by heat-assisted laser annealing*”, Ext. Abst. of Int. Meeting for Future Electron Devices, Kansai (2005 IMFEDK, Kyoto, Apr. 11-13, 2005), pp. 135-136.
- 69) T. Eto and K. Shibahara, “*Accuracy of SIMS depth profiling for sub-keV As⁺ implantation*”, Jpn. J. Appl. Phys., **44** (2005) 2433-2436.
- 70) E. Takii, T. Eto, K. Kurobe, and K. Shibahara, “*Ultra shallow junction formation by green-laser annealing with light absorber*”, Jpn. J. Appl. Phys., **44** (2005) L756-L759.
- 71) K. Shibahara, “*Benefits of heat-assist for laser annealing*”, Ext. Abst. of Int. Workshop on Junction Technology, (IWJT'05, Osaka, Jun. 6-7, 2005), pp. 53-54, (**Invited**).
- 72) K. Hosawa, K. Matsumoto, and K. Shibahara, “*Anomalous doping profile in heavily doped Ge*”, Extended Abstracts of Int. Workshop on Junction Technology, (IWJT'05 ,Osaka, Jun. 6-7, 2005), pp. 39-40.
- 73) K. Sano, M. Hino, N. Ooishi, and K. Shibahara, “*Workfunction tuning using various impurities for fully silicided NiSi*”, Jpn. J. Appl. Phys., **44** (2005) 3774-3777.

- 74) A. Matsuno, E. Takii, T. Eto, K. Kurobe, and K. Shibahara, “*Merits and demerits of light absorbers for ultra shallow junction formation by green laser annealing*”, Nucl. Instr. and Meth. B, **237** (2005) 136-141.
- 75) A. Matsuno, and K. Shibahara, “*Function of phase switch layer for ultra shallow junction formation by green laser annealing*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'05, Kobe, Sep 13-15, 2005), pp.914-915.
- 76) K. Shibahara, A. Matsuno, E. Takii, and T. Eto, “*Green laser annealing with light absorber*”, 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors - RTP 2005 (Santa Barbara, Oct. 4-7) pp.101-104.
- 77) K. Sano, T. Hosoi, and K. Shibahara, “*Importance of heat-up ramp rate for palladiumsilicide fully-silicided-gate structure formation*”, 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors - RTP 2005 (Santa Barbara, Oct. 4-7) pp. 145-148.
- 78) K. Kurobe, Y. Ishikawa and K. Shibahara, “*Sheet resistance reduction and crystallinity improvement in ultrashallow n⁺/p junctions by heat-assisted excimer laser annealing*”, Jpn. J. Appl. Phys., **44** (2005) 8391-8395.
- 79) T. Hosoi, K. Sano, M. Hino, A. Ohta, K. Makihara, H. Kaku, S. Miyazaki, and K. Shibahara, “*Characterization of Sb-doped fully-silicided NiSi/SiO₂/Si MOS structure*”, 2005 Int. Semiconductor Device Res. Symp. Proceedings (ISDRS 2005, Bethesda, Maryland, USA, Dec. 7-9, 2005) pp. WP-4-05-1-WP-4-05-2.
- 80) K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara and H. Sunami, “*Application of arsenic plasma doping in three-dimensional MOS transistors and the doping profile evaluation*”, Jpn. J. Appl. Phys., **44** (2005) 2273-2278.
- 81) T. Tanaka, S. Watanabe, K. Shibahara, S. Yokoyama and T. Takagi, “*Plasma-based ion implantation sterilization technique and ion energy estimation*”, J. Vac. Sci. Technol. A, **23** (2005) 1018-1021.

- 82) K. Shibahara, “*Metal gate technology for 45nm and beyond*”, Proceedings of 2006 Int. Symp.on VLSI Technology, Systems, and Applications (VLSI-TSA 2006, Hsinchu, Taiwan, Apr. 24-26, 2006) pp. 105-106, (**Invited**).
- 83) K. Shibahara, A. Matsuno, M Hino, and K. Kurobe, “*Mo gate deformation induced by laser annealing process*”, Proceedings of 2006 Int. Symp.on VLSI Technology, Systems, and Applications (VLSI-TSA 2006, Hsinchu, Taiwan, Apr. 24-26, 2006) pp. 50-51.
- 84) K. Shibahara, T. Eto, and K. Kurobe, “*Merits of heat-assist for melt laser annealing*”, IEEE Trans. Electron Devices, **53** (2006) 1059-1064.
- 85) T. Fukunaga, K. Hosawa, T. Hosoi and K. Shibahara, “*Xe preamorphization implantation for transient enhanced diffusion suppression of As in Ge substrate*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'06, Yokohama, Sep. 13-15, 2006) pp. 452-453.
- 86) T. Hosoi, K. Sano, K. Hosawa, and K. Shibahara, “*Pd₂Si fully-silicided gate: kinetics of silicide formation and workfunction tuning*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'06, Yokohama, Sep. 13-15, 2006) pp. 218-219.
- 87) A. Matsuno and K. Shibahara, “*Effects of pulse duration on the formation of ultra shallow junction formed by an excimer laser anneal method*”, Jpn. J. of Appl. Phys., **45** (2006) 8537-8541.
- 88) A. Ohta, H. Yoshinaga, H. Murakami, D. Azuma, Y. Munetaka, S. Higashi, S. Miyazaki, T. Aoyama, K. Kosaka, and K. Shibahara, “*Evaluation of chemical structures and work function of NiSi near the Interface between nickel silicide and SiO₂*”, Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'06, Yokohama, Sep. 13-15, 2006), pp. 216-217.
- 89) M. Tanaka, T. Hosoi and K. Shibahara, “*Issues for Pd₂Si and NiSi fully silicided gate formation*”, Conf. Digest of The 2007 International Meeting for Future of Electron Devices, Kansai (2007 IMFEDK, Osaka, Japan, April 23-24, 2007) pp. 39-41.

- 90) T. Hosoi, K. Sano, K. Hosawa, and K. Shibahara, “*Formation kinetics and workfunction tuning of Pd₂Si fully silicided metal gates*”, Jpn. J. Appl. Phys., **46** (2007) 1929-1933.
- 91) K. Shibahara and N. Maeda, “*Gate-extension overlap control by Sb tilt implantation*”, IEICE Trans. Electron., **E90-C** (2007) 973-977.
- 92) K. Shibahara, T. Eto and T. Fukunaga, “*Dual-Pearson parameter extraction for In tilt implantation*”, Ext. Abs. the 7th International Workshop on Junction Technology 2007 (IWJT'07, Kyoto, Japan, June 8-9, 2007) pp. 25-26.
- 93) T. Yamashita, Y. Nishida, T. Okagaki, Y. Miyagawa, J. Yugami, H. Oda, Y. Inoue, and K. Shibahara, “*Study of stress from discontinuous SiN liner for fully-silicided gate process*”, Ext. Abst. of the 2007 Int. Conf. on Solid State Devices and Materials (SSDM'07, Tsukuba, Japan, Sep. 19-21, 2007) pp. 870-871.
- 94) K. Shibahara, T. Eto and T. Fukunaga, “*Universality of Pearson parameters extracted for In tilt implantation*”, Proceedings of 2007 Korea-Japan Joint Workshop on Advanced Semiconductor Processes and Equipments, (ASPE'07, Oct. 4-6, 2007, Busan, Korea) pp. 215-217.
- 95) T. Hosoi, K. Shibahara, M. Song, and K. Furuya, “*In-situ TEM observation of silicide formation and dopant segregation in Ni fully silicided gates*”, Proc. of Fifth Int. Symp. on Control of Semiconductor Interfaces (ISCSI-V, Tokyo, Japan, November 12-14, 2007) pp. 147-148.
- 96) T. Yamashita, Y. Nishida, T. Okagaki, Y. Miyagawa, J. Yugami, H. Oda, Y. Inoue, and K. Shibahara, “*Stress from discontinuous SiN liner for fully silicided gate process*”, Jpn. J. App. Phys., **47** (2008) 2569-2574.
- 97) T. Hosoi, K. Sano, A. Ohta, K. Makihara, H. Kaku, S. Miyazaki, and K. Shibahara, “*Interface properties and effective work function of Sb-predoped fully silicided NiSi gate*”, Surface and Interface Analysis, **40** (2008) 1126-1130.

- 98) T. Yamashita, Y. Nishida, K. Eikyu, H. Oda, Y. Inoue, and K. Shibahara, “*Threshold voltage modulation using N_2^+ implantation into substrate for Ni fully silicided gate/high-k NMOS*”, IEEE Electron Device Lett., **29** (2008) 1163-1166.
- 99) K. Shibahara, T. Fukunaga, and Takuji Hosoi, “*Ge shallow junction formation with preamorphizing technique*”, Proceedings of 2008 Korea-Japan Joint Workshop on Advanced Semiconductor Processes and Equipments, (ASPE’08, Oct. 9-11, 2008, Shikabe, Japan) pp. 163-166.
- 100) T. Hosoi, A. Ohta, S. Miyazaki, H. Shiraishi, and K. Shibahara, “*Photoemission study of fully silicided Pd_2Si gates with interface modification induced by dopants*”, Appl. Phys. Lett., **94** (2009) 192102 (3 pages).
- 101) M. Terai, T. Hase, K. Shibahara, H. Watanabe, “*Effects of Si/Ni composition ratio of Ni_xSi_y gate electrode and Hf/Si composition ratio of Hf-based high-k insulator on threshold voltage controllability and mobility of metal-oxide-semiconductor field-effect transistors*”, Jpn. J. Appl. Phys., **49** (2010) 036504 (7 pages).
- 102) Y. Nishida, K. Eikyu, A. Shimizu, T. Yamashita, H. Oda, Y. Inoue, K. Shibahara, “*Temperature coefficient of threshold voltage in high-k metal gate transistors with various TiN and capping layer thicknesses*”, Jpn. J. Appl. Phys., **49** (2010) 04DC03 (5 pages).