## V. ION IMPLANTATION INTO 3C-SiC GROWN LAYERS AND APPLICATION TO MOSFETs

A selective doping technique is indispensable in fabrication of electronic devices especially for IC (integrated circuits). There are two major techniques for selective doping, namely, diffusion and ion implantation methods. Both methods are popular for a Si process. However, in the case of SiC the diffusion method is hard to apply, because the diffusion coefficients of impurities in SiC are very low. Campbel and Chang fabricated junction-gate FETs of $\alpha$-SiC using a diffusion technique [1]. They reported that diffusion of Al into $\alpha$-SiC required temperatures from 1800° C to 2100° C. Moreover, a special masking technique utilizing SiC was necessary. Thus, the diffusion method seems to be not practical for SiC. Ion implantation into $\alpha$-SiC was attempted by many investigators [2–6]. Marsh investigated the activation of implanted impurities using various dopants [2]. Though the implantation of donor impurities such as N, P, Sb and Bi was successful, samples implanted with acceptors were high resistive even after annealing and the acceptors could not be activated. They explained that deep donor-type defects induced by the implantation prevented the activation of the implanted acceptors. Concerning 3C-SiC, Kalinina et al. [7] reported a successful fabrication of p-n junction diodes by implantation of Al, however, they did not describe details of investigation. Though Kondo et al. [8] attempted hot implantation (specimens were intentionally heated during implantation) in addition to the standard implantation, the activation was unsuccessful. Edmond et al. [9] reported successful fabrication of p-n junction diodes by hot implantation of Al into undoped layers without annealing. The crystal growth methods of these two groups are similar to that of this investigation. The difference in their investigations is not clear.
In this investigation, implantation of $N_2^+$ and $P^+$ was attempted. The electrical characteristics of implanted layers were evaluated changing annealing temperatures. Planar-type p-n junction diodes were fabricated using the implantation technique. The first successful fabrication of n-channel inversion-type MOSFETs is mentioned. The MOSFETs were fabricated by the combination of ion implantation and thermal oxidation techniques which are ordinary in the Si process.

### 2. Activation of implanted donors

Ion implantation of $N_2^+$ and $P^+$ was carried out into B-doped grown layers. High resistive ($\rho \geq 200\ \Omega$·cm) B-doped layers were suitable for characterization of thin $n^+$ layers formed by implantation of donors. The thickness of the B-doped grown layers was about 6 $\mu$m. APD-free grown layers on 2° off substrates were used. Samples were tilted at 7°

during the implantation to avoid a channeling effect. The current density of an ion beam was lower than 0.25 $\mu$A/cm$^2$. Therefore, heating by the beam during the implantation was negligible [10]. The conditions of the ion implantation were listed in Table 1. The implantation was carried out by successive two steps to improve the uniformity of implanted impurities. The first implantation was high dose with high energy and the second was low dose with low energy. Figure 1 shows a calculated profile of implanted P using the projected average range and projected standard deviation in the literatures [11–13] for a total dose of $1.3\times10^{15}$ cm$^{-2}$ (condition 1 in Table 1). In the case of condition 2, the total dose was decreased to 30% of that in condition 1 with the same energy. $N_2^+$ implantation with a total dose of $1.95\times10^{14}$ cm$^{-2}$ (condition 3) corresponds to $N^+$ implantation with a dose of $3.9\times10^{14}$ cm$^{-2}$ which is the same dose level as condition 2. The energy of the $N_2^+$ implantation was decided to have the nearly same impurity profile [13] as in $P^+$ implantation of condition 2. After the implantation samples were annealed in
Ar atmosphere for 30 min. The samples were heated by RF inductive heating. By SIMS analysis the annealed specimen showed almost the same depth profile of implanted P as that with without annealing by SIMS analysis. Figure 2(a) shows a RHEED halo pattern of an as-implanted sample. The ion implantation was carried out under condition 1 ($P^+$, total dose: $1.3\times10^{15}$ cm$^{-2}$). The halo pattern indicates that the implanted layer was amorphous. Figure 2(b) shows a RHEED pattern of the sample after annealing at 800° C. Recrystallization to a single crystal was clearly observed. Annealing temperature was changed up to 1300° C. However, no significant difference in RHEED patterns compared with Fig. 2(b) was observed. Samples implanted under condition 2 ($P^+$, total dose: $3.9\times10^{14}$ cm$^{-2}$) showed similar results. The implanted samples could be told from not implanted samples with naked eyes by noticing a slight difference in colors. The refractive index of the implanted layers changed by amorphization and interference took place. The difference in colors vanished by annealing. Sheet resistance of the implanted layers was evaluated by the four-point probe method or by van der Pauw method. Si substrates of the specimens for van der Pauw measurement were removed by a mixed solution of $HNO_3$ and HF before the measurement to avoid errors due to current conduction through the substrates. N-type conduction was confirmed for both the $P^+$ and $N_2^+$ implanted layers by van der Pauw method. As shown in Fig. 3, the sheet resistance monotonously decreased as annealing temperature increased and it reached to about $10^3$ Ω/□ by annealing at about 1350° C. Electrical activation rates were estimated by van der Pauw measurement. The electrical activation rate was defined as the ratio of sheet carrier concentration and total dose. The electrical activation rates were improved by raising annealing temperatures as shown in Fig. 4. The $P^+$ implanted layer with a total dose of $3.9\times10^{14}$ cm$^{-2}$ (condition 2) gave the higher electrical activation rates than

those for a total dose of $1.3\times10^{15}$ $cm^{-2}$ (condition 1). The $N_2^+$ implanted layers gave the

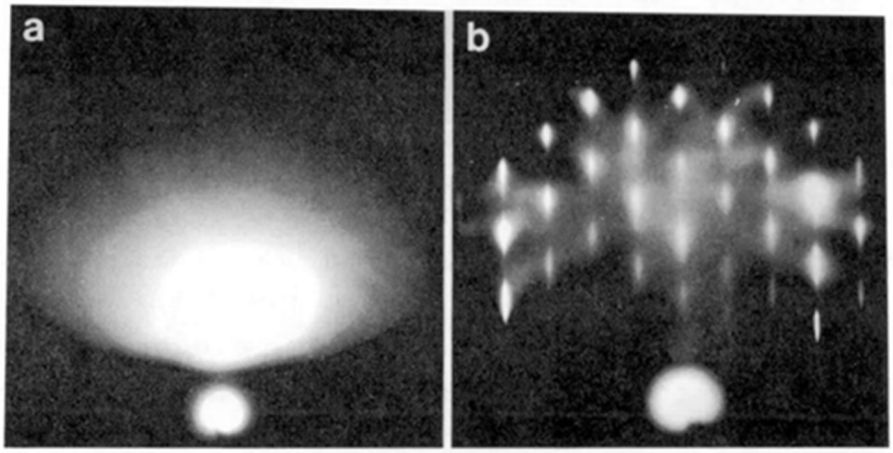


Fig.2 RHEED patterns of $P^+$ implanted layers. (a)Before and (b)after annealing at 800°C.

…higher electrical activation rates than the $P^+$ implanted layers, which is similar to implantation into 6H-SiC [2]. Bridge-type specimens were fabricated by the $P^+$ implantation to carry out the standard Hall measurement and to investigate electrical anisotropy in the implanted layers. Such specimens were fabricated by a selective implantation utilizing a deposited $SiO_2$ film as a mask. The implantation was carried out under condition 2. Concerning conditions 1 and 3 the standard Hall measurement was not carried out yet. The electrical activation rates obtained by the standard Hall measurement well agreed with those obtained by van der Pauw measurement. The electron mobility obtained by van der Pauw method was about 30 $cm^2/Vs$ in all cases. The electron mobility obtained by the standard Hall measurement showed electrical anisotropy similar to the undoped grown layers. $\mu\,/\!/$ and $\mu\perp$ were about 50 and 25 $cm^2/Vs$, respectively.

### 3. Fabrication of p-n junction diode

Planar-type p-n junction diodes were fabricated using the ion implantation technique. Figure 5 shows the structure of fabricated diodes. An Al-doped p-layer was grown on a 2° off p-Si substrate. Typical hole concentration, hole mobility and resistivity of the Al-doped layer were $3.5\times10^{17}$ $cm^{-3}$, 32 $cm^2/Vs$ and 0.56 Ω·cm, respectively. $P^+$ implantation with a total dose of $3.9\times10^{14}$ $cm^{-2}$ or $N_2^+$ with a total dose of $1.95\times10^{14}$ $cm^{-2}$ was carried out to obtain n-layers. Deposited $SiO_2$ of 500 nm in thickness was used as a mask for the implantation. Annealing temperatures were 1100° C, 1200° C and 1300° C. Annealing

time was fixed at 30 min. Finally ohmic contacts were formed using Al and AuGa for n-SiC and p-Si, respectively. The area of the fabricated diodes was $7.1\times10^{-4}$ cm$^2$. Current-voltage characteristics of the $P^+$ and $N_2^+$ implanted diodes were shown in Figs. 6(a) and (b), respectively. Both the $P^+$ and $N_2^+$ implanted diodes showed similar results. Rectification of the diodes annealed at 1100° C and 1200° C was superior to those…

The electrical activation rate increased abruptly when annealing temperatures exceeded 1300° C. This change was attributed to the transition from an n-layer to an $n^+$-layer due to increased electrical activation. The best ideal diode factor of 3.8 was achieved at an annealing temperature of 1100° C for both $P^+$ and $N_2^+$ implanted diodes. Capacitance-voltage characteristics showed small variation initially, but increased with higher annealing temperatures. The diodes had p-i-n structures, and the i-layer thickness decreased with higher annealing temperatures. $N_2^+$ implanted diodes exhibited larger capacitance and variation due to higher electrical activation rates compared to $P^+$ implanted diodes.

## 4. Fabrication of MOSFETs

MOSFETs were fabricated using ion implantation. A schematic cross-section is shown in Fig. 8. A B-doped p-SiC channel layer of 2 $\mu$m thickness was grown on undoped n-SiC with a thickness of 7 $\mu$m. Due to lattice mismatch between Si and SiC, a thicker layer is necessary to reduce defects and improve device characteristics. Source and drain were formed by ion implantation of $P^+$ using deposited $SiO_2$ with a thickness of 500 nm as a mask. The implantation was carried out under condition 1 in Table 1. Annealing was performed in an IR radiative heating furnace.

The gate insulator was formed by thermal oxidation of SiC at 1050° C using dry oxygen for 6 hours. The thermal oxide film was confirmed to be $SiO_2$ and inversion was verified under illuminated conditions. Electrical resistivity and breakdown electric field of $SiO_2$ were $8.5\times10^{15}$ Ω·cm and $2.5\times10^6$ V/cm, respectively. The gate oxide thickness was about 60 nm, with gate length and width of 20 μm and 500 μm, respectively. Aluminum was used for gate electrodes and ohmic contacts, without alloying. A top view of the fabricated MOSFET is shown in Fig. 9. Current-voltage characteristics of the FET at 310 K are discussed, noting that the sample was not illuminated. Inversion-type MOSFET action was achieved, with observed kinks in the saturation region, a feature of SOI MOSFETs. The MOSFETs were fabricated on a high resistive B-doped p-layer, and their characteristics were considered to show SOI-like features. In Al-$SiO_2$-SiC MOS diodes, inversion occurred only under illumination due to low intrinsic carrier concentration (~10 cm$^{-3}$ at 300 K) of 3C-SiC. However, the MOSFETs operated without illumination, with electrons supplied from the source. The effective mobility of the FET was estimated in the linear region, where drain

voltage was lower than the voltage at the beginning of the kink. The ideal characteristics of MOSFETs in the linear region are given by:

[ I_d = ¥left(¥frac{W}{L}¥right) ¥mu_n C_0 ¥left[(V_g - V_{th})V_d - ¥frac{V_d^2}{2}¥right], ¥quad (1) ]

where ( I_d ) is drain current, ( W ) is gate width, ( L ) is gate length, ( ¥mu_n ) is electron mobility, ( V_g ) is gate voltage, ( V_{th} ) is threshold voltage, and ( V_d ) is drain voltage. The ratio ( W/L ) is 25, and the value of ( C_0 ) is $5.75 \times 10^{-8}$ F/cm², based on an investigation of the Al-$SiO_2$-SiC system. ( ¥mu_n ) and ( (V_g - V_{th}) ) were adjusted to match measured ( I_d )-( V_d ) characteristics.

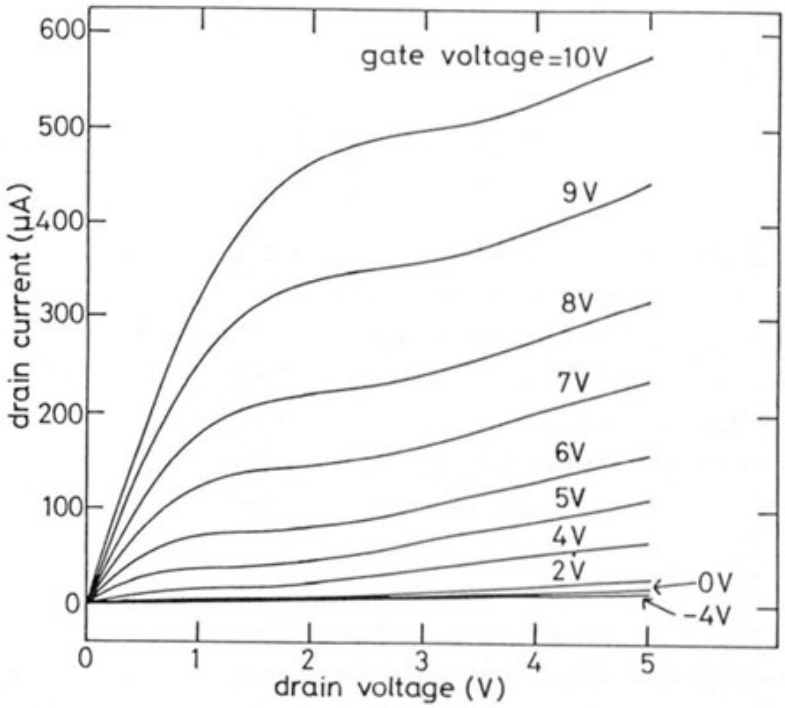


Fig. 10 Current-voltage characteristics of the MOSFET at 310K.

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