VI. CVD GROWTH ON 6H-SiC(0001)

1. Introduction

In the former chapters 3C-SiC grown on Si was treated. In this chapter growth on 6H-SiC(0001) is the main subject. Many investigators carried out homoepitaxial growth of 6H-SiC at temperatures of about 1800°C, and applications to blue LED's[1,3] and bipolar transistors[4] were already reported. 6H-type is the most popularly obtainable polytype at high temperatures over 1800°C[5] even in the case of growth without substrates. Such high temperatures are believed to be suitable also for CVD growth. However, growth at lower temperatures reminds us of two interesting meanings. One concerns possibility of utilizing 6H-SiC(0001) as a substrate of 3C-SiC, and the other is control of polytypes of CVD grown layers.

As explained in the first chapter, structures of all polytypes of SiC are expressed by stacking sequences in the [0001] direction concerning layers of close packed atoms. 3C- and 6H- type have the stacking sequences of *ABC* and *ABCACB*, respectively. Ideally every sequence which consists of '*A*', '*B*' and '*C*' is permitted as far as the sequences does not include repetition of the same layer such as '*AA*', '*BB*' or '*CC*'. And so, ideally we can draw a structure of 3C-SiC grown on 6H-SiC with stacking sequence of *ABCABCABCACBABCACB*... In the case of growth at relatively low temperatures, 3C-type is most popularly obtained. Therefore, growth of 3C-type on 6H-substrates is expected at low temperatures.

When crystal growth begins by random nucleation, polytypes of the grown crystals are explained by the stability connected with temperatures. However, in the case of epitaxial growth, the transmission of the stacking information from substrates is considerable. Therefore, it is interesting whether the polytypes of epitaxially grown layers can be varied by controlling temperature and substrates. In this investigation, CVD growth was

carried out at temperatures in the range of 1350-1500°C, and "control of substrates" was realized by introducing off orientation.

2. CVD growth

Used substrates were all 6H-SiC(0001) Si-faces grown by Acheson method. Because naturally formed flat faces of crystals grown by Acheson method are usually (0001) Si-faces or $(000\bar{1})$ C-faces, and surface flatness of CVD and LPE grown layers on (0001) Si-faces was reported to be superior to that on $(000\bar{1})$ C-faces[6,8]. The (0001) Si-face was selected utilizing the difference in oxidation rates between these two faces[9]. Two types of substrates were prepared. One was a natural flat face and the other was a face angle-lapped with carborundum powder. Hereafter the former and the latter are called natural and lapped faces, respectively. Both faces were polished with diamond paste as finishing.

For CVD growth the same system was used as 3C-SiC on Si. Since growth temperature was higher than growth on Si, small size susceptors were used to prevent over-heating of the wall of a reaction tube. Figure 1 shows a temperature program of the CVD growth. Before the growth, etching of substrates by gaseous HCl or molten KOH was carried out. Etching temperatures by gaseous HCl and molten KOH were 1500°C and around 450°C, respectively. Source gases were SiH_4 and C_3H_8. Growth temperatures were in the range of 1350°C-1500°C. A typical growth rates was about 2μm/hr.

Figure 2 shows a typical surface morphology of the grown layers on natural faces. A mosaic pattern which consists of step-like or groove-like boundaries was observed. Such morphology was already reported[7,10,11]. Figure 3 shows a SEM photograph of pits on the surface of the grown layers etched by molten KOH. The etch pits give us the following information. Since the pits have a triangular shape, the grown layers are 3C-SiC[12-14]. The apices of the triangles of the pits point 180° opposite

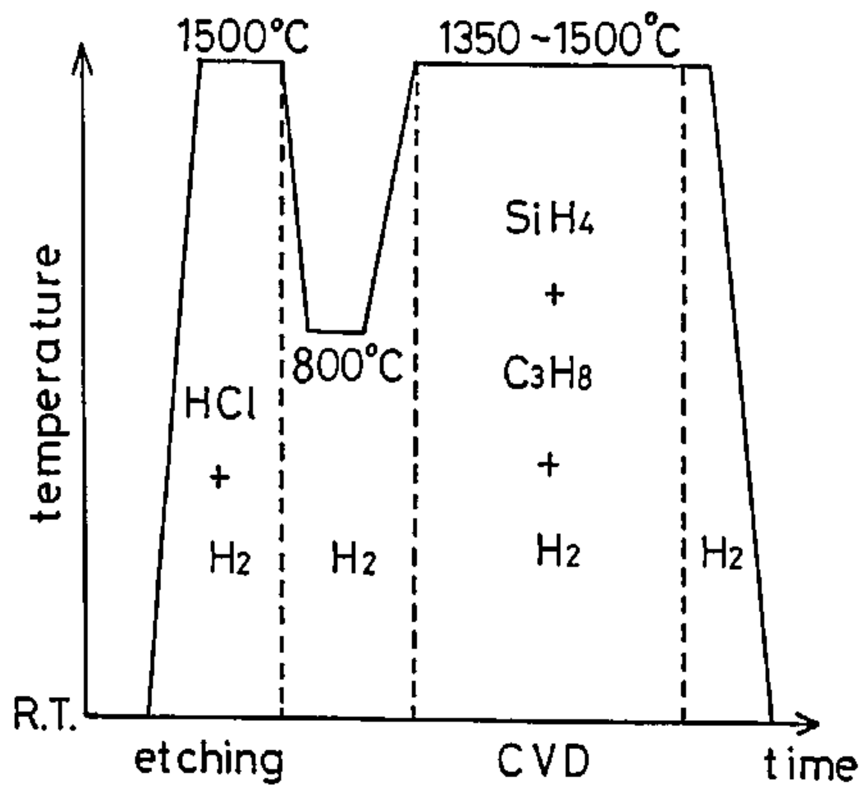


Fig.1 Temperature program of CVD growth procedure.

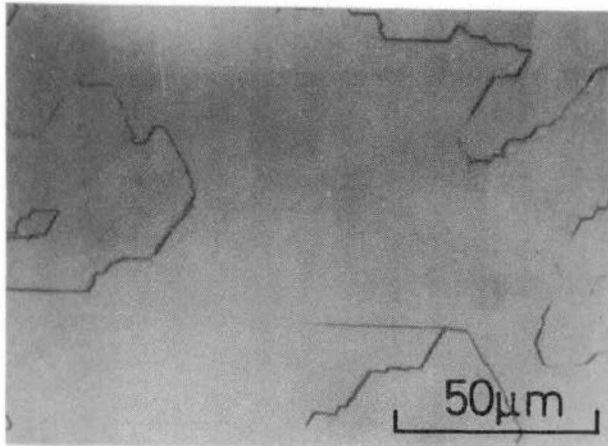


Fig.2 Nomarski microphotograph of the surface of a grown layer on a natural face. Boundarylike grooves are observed.

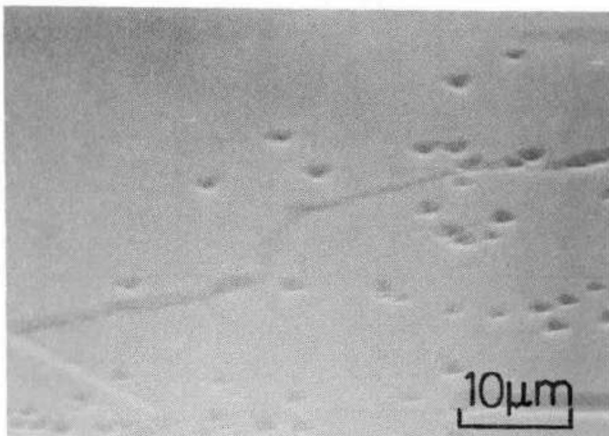


Fig.3 SEM microphotograph of the etched surface of a grown layer on a natural face. Triangular pits are observed.

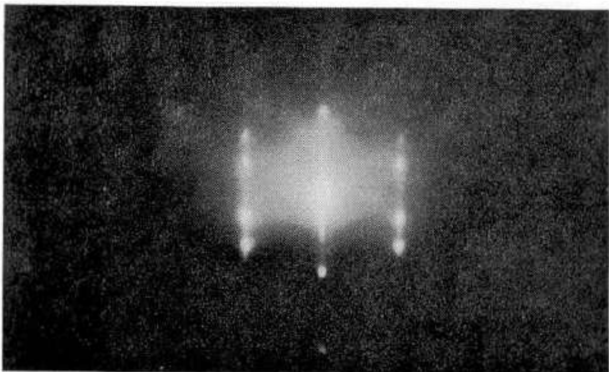


Fig.4 $\langle 100 \rangle$ (or $\langle 2\bar{1}\bar{1}0 \rangle$) azimuth RHEED pattern of a grown layer on a natural face. 3C-SiC containing twinning was grown.

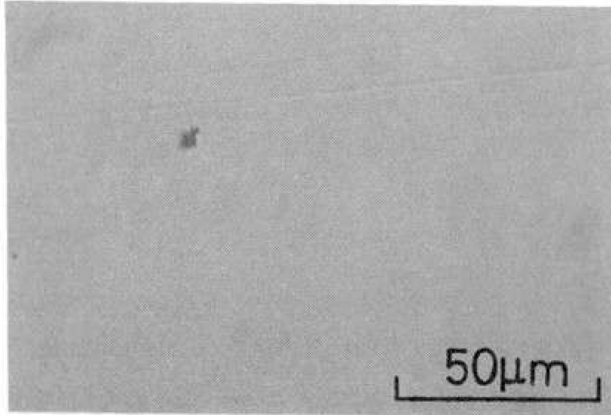


Fig.5 Nomarski microphotograph of the surface of a grown layer on a lapped face. Observed straight lines are scratches formed by polishing.

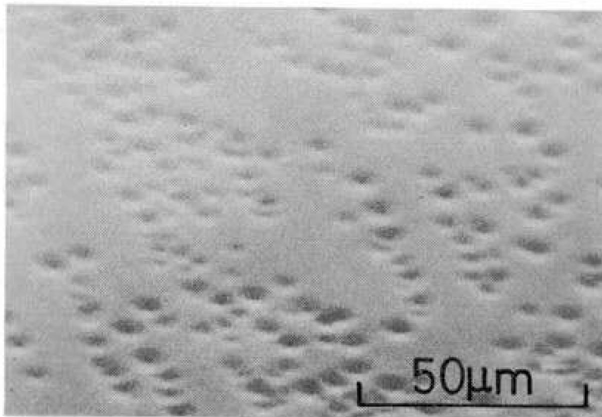


Fig.6 SEM microphotograph of the etched surface of a grown layer on a lapped face.

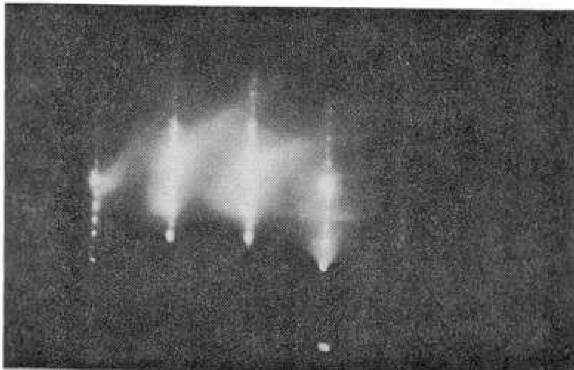


Fig.7 $\langle 100 \rangle$ (or $\langle 2\bar{1}\bar{1}0 \rangle$) azimuth RHEED pattern of a grown layer on a lapped face. Single crystalline 6H-SiC was grown.

directions in the neighboring regions separated by the boundaries, which means that the boundaries were twin-boundaries. In short, the grown layers on natural faces were 3C-SiC containing twinning, which was also confirmed by RHEED as shown in Fig.4. Details of interpretation of RHEED patterns are mentioned in the next section. Variation of the Si/C ratio was no help for elimination of twinning. By optimizing etching conditions, the intervals between the boundaries were slightly widened.

The (0001)Si face was lapped and polished as mentioned above to introduce off orientation. Figure 5 shows a typical surface morphology of the grown layers on lapped faces. A very smooth surface was obtained. As shown in Fig.6 pits formed by molten KOH etching had a circular shape and could not be directly utilized for identification of polytypes. No boundary-like structures were observed on the etched surface. The RHEED patterns shown in Fig.7 indicated that the grown layers were single crystalline 6H-SiC.

Single crystalline 6H-SiC was obtained on lapped faces in the range of growth temperatures from 1400°C to 1500°C. These temperatures are very low compared with an ordinary growth temperature of 1800°C for 6H-SiC. When the temperature was 1350°C, the grown layers on both natural and lapped faces were 3C-SiC containing twinning as explained below. The surface morphology of the grown layers on natural faces was similar to that grown at temperatures over 1400°C containing the boundaries. The grown layers on lapped faces showed flat surfaces as shown in Fig.8. However, RHEED patterns for the grown layers on both natural faces and lapped faces were similar to Fig.4 and indicated that the grown layers were 3C-SiC containing twinning.

There were many differences between growths at 1350°C and at 1400-1500°C in addition to the difference in polytypes of the grown layers. Figure 9 shows droplets observed on the surfaces of SiC grown at temperatures over 1400°C. The RHEED pattern of an as-grown surface with droplets showed spots due to Si. After removing the droplets with a mixed solution of HF and HNO_3, the spots due to Si in the RHEED patterns disappeared. The droplets

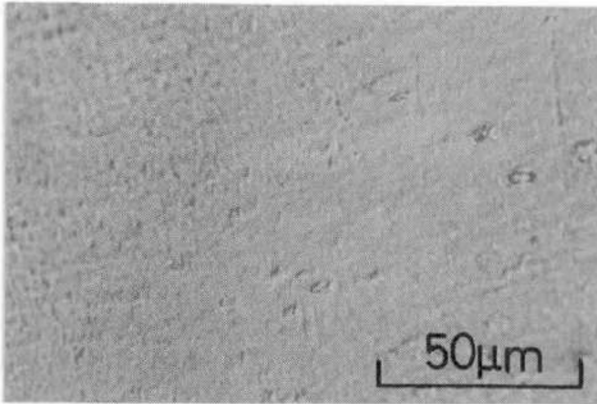


Fig.8 Nomarski microphotograph of the surface of a grown layer on a lapped face. Growth temperature was reduced to 1350°C.

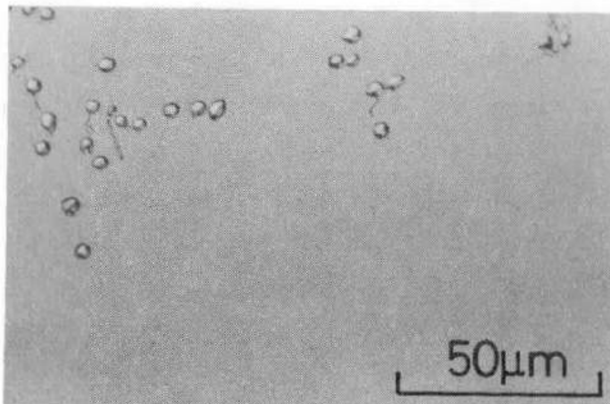


Fig.9 Si droplets observed on SiC grown at temperatures higher than the melting point of Si.

could be eliminated by decreasing the Si/C ratio. Therefore, the droplets are considered to originate from excessively supplied Si cohered as molten droplets during growth at temperatures higher than the melting point of Si. The melting point of Si is 1420°C and is higher than 1400°C. In the used system a Si wafer put on a susceptor melted over 1400°C. The difference of 20°C is an error due to temperature measuring method mentioned in Chapter 2.

Table 1 shows the relationship between the Si/C ratio and surface flatness of the grown layers on lapped faces. At 1350° the Si/C ratio should be rigidly optimized to obtain a flat surface. However, at temperatures over 1400°C a flat surface was obtained in the wide range of the Si/C ratio. These results about the droplets and the Si/C ratio are explained as follows. At temperatures over the melting point of Si, since stable Si-Si bonding cannot exist, excessively supplied Si does not prevent growth of SiC. However, at temperatures under the melting point of Si, excessively supplied Si forms crystalline Si and growth of SiC is affected similarly to the case of growth on Si mentioned in Section II-4-1. Thus, the growth mechanism at 1350°C is considered to be different from that at temperatures over the melting point of Si.

The relationship between the growth conditions and polytypes of the grown layers is shown in Table 2. The mechanism which decides polytypes of the grown layers includes two important factors of the orientation of substrates and growth temperatures. In the range of 1400°C-1500°C polytypes were varied by the orientation of substrates. Figure 10 shows the relationship between the polytypes of the grown layers and the magnitude and the direction of the off orientation. The off angle and the direction were measured using an X-ray diffractometer. When the off angle was larger than 1.5°, 6H-SiC was grown homoepitaxially. This result is explained in relation to surface steps introduced by the off orientation. We assume that fundamentally epitaxial growth takes place inheriting the stacking information of atoms nearby the surface. When the polished natural face is used, the

Si/C RATIO AND SURFACE MORPHOLOGY

Si/C \ Ts	1350°C	1400-1500°C
<0.03	---	good
0.03-0.3	---	good*
0.32	bad	good*
0.56	good	good*
0.74	bad	---

Ts: growth temperature
---: not yet tried
*: Si droplets were observed.

Table 1 Relationship between the Si/C ratio and surface morphology of grown layers.

GROWTH CONDITIONS AND POLYTYPES

sub. \ Ts	1350°C	1400-1500°C	>1800°C
natural face	3C(twin)	3C(twin)	6H*
lapped face	3C(twin)	6H	---

*: by Nishino et al.[7]
Ts: growth temperature, sub.: substrates
---: not yet tried

Table 2 Variation in polytypes of grown layers due to the change of growth temperatures and orientations of substrates.

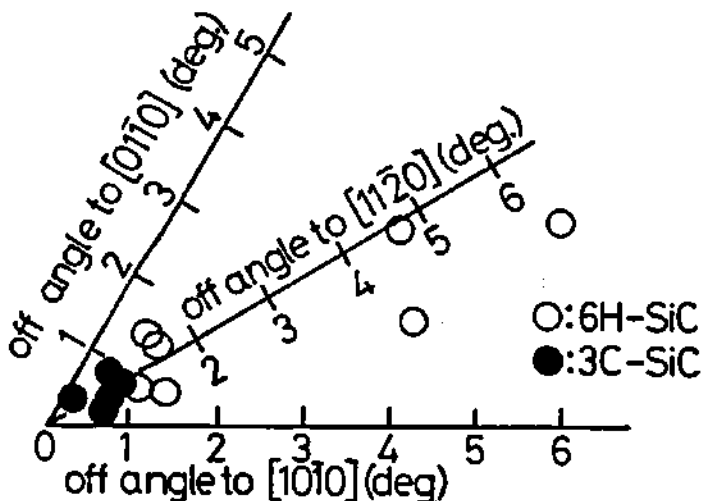


Fig.10 The relationship between polytypes of grown layers and the off orientation of substrates.

density of surface steps is very low. Therefore, growth mainly takes place on the flat surface not at the steps. Then, arrived atoms on the surface inherit the stacking information of the atoms that locate just under the surface.

Even on the natural face which has a very low offset angle from (0001), there are steps in a macroscopic view point. Hence, the surface of the 6H-SiC(0001) face can be divided into two parts. In one part the surface is occupied by the atoms belonging to *ABC* of the former half of the stacking sequence of *ABCACB*, and in the other part by the atoms belonging to *ACB* of the latter half. On the *ABC* part 3C-SiC grows in accordance with the stacking sequence of *ABC*, and on the other part in accordance with *ACB* as shown in Fig.11(a). In other words on the natural face of 6H-SiC twin crystals of 3C-SiC grow.

As the off angle becomes larger, the density of the surface steps becomes larger. Then atoms easily reach to the steps by migration. In this case, epitaxial growth takes place inheriting the stacking information around the steps as shown in Fig.11(b). Hence, 6H-SiC layers were obtained on off-oriented substrates. Even on natural faces 6H-SiC layers were obtained at 1800°C[7]. There are two mechanisms which can explain the result. One is that 6H-SiC is stable at temperatures over 1800°C. And the other is explained as follows based on the model mentioned above. At very high temperatures surface migration becomes active. Therefore, even if the density of steps is low, atoms can reach to the steps and 6H-SiC can grow epitaxially at high temperatures. Powell and Will reported epitaxial growth of 6H-SiC at very low temperatures under 1400°C on the faces perpendicular to {0001} C-faces.[13] Their investigation corresponds to growth on substrates with an off angle of 90°.

At 1350°C the introduction of off orientation did not give rise to variation in polytypes. As discussed above the growth mechanism at 1350°C is different from that at temperatures higher than the melting point of Si. And the polytype of the grown layers is probably decided in a different way.

Fig.11 Model of (a) growth of twinned 3C-SiC on well oriented 6H-SiC(0001) and (b) homo-epitaxial growth on off oriented 6H-SiC(0001).

Fig.12 Theoretical <210> (or $\langle 10\bar{1}0 \rangle$)azimuth RHEED pattern for all polytypes of SiC. Where n is a number of layers in the repeat distance.

3. Identification of polytypes

(RHEED observation)

The most fundamental method to identify the structure of crystals is a diffraction technique. The examples of identification by X-ray oscillation[15], TED(transmission electron diffraction)[11,16] and Kikuchi lines in electron diffraction patterns[17] were reported. In this work, structure identification was carried out by RHEED observation. This method is convenient for thin grown layers. Moreover, sample preparation and interpretation of results are easy.

To obtain theoretical RHEED patterns, reciprocal vectors, structural factors and double reflection should be taken into account. The detail of calculation is mentioned in an appendix. $\langle 1\bar{1}0\rangle$ and $\langle 210\rangle$*) azimuth patterns of SiC(0001) in Fig.12 are common to all polytypes. However, $\langle 100\rangle$ and $\langle 110\rangle$*) azimuth patterns are peculiar to each polytype. $\langle 100\rangle$ azimuth patterns for 3C, 6H and 15R types are shown in Figs.13(a)-(c). For hexagonal polytypes $\langle 100\rangle$ patterns are symmetrical, but those for 3C and rhombohedral polytypes are asymmetrical. When 3C-SiC contains twinning the pattern is synthesized by Fig.13(a) and its mirror image as shown in Fig.14.

*) $\langle \bar{1}10\rangle$ and $\langle 210\rangle$ directions correspond to $\langle 10\bar{1}0\rangle$. $\langle 100\rangle$ and $\langle 110\rangle$ directions correspond to $\langle 2\bar{1}\bar{1}0\rangle$. See an appendix for detail.

To apply this method to practical identification, spot patterns must be observed. However, surfaces of natural faces and grown layers are usually so flat that streak patterns are obtained. To obtain a spot pattern intentionally roughness should be introduced onto the surface. In this work, lapping and molten KOH etching were attempted. Figure 15 shows a $\langle 100\rangle$ azimuth pattern of a 15R-SiC (0001) substrate. The surface of the sample was lapped with carborundum. By lapping the surface was roughen and partly changed to poly-crystalline. Sometimes the surface became too rough for RHEED observation. To obtain adequate roughness was very difficult in this method. For grown layers

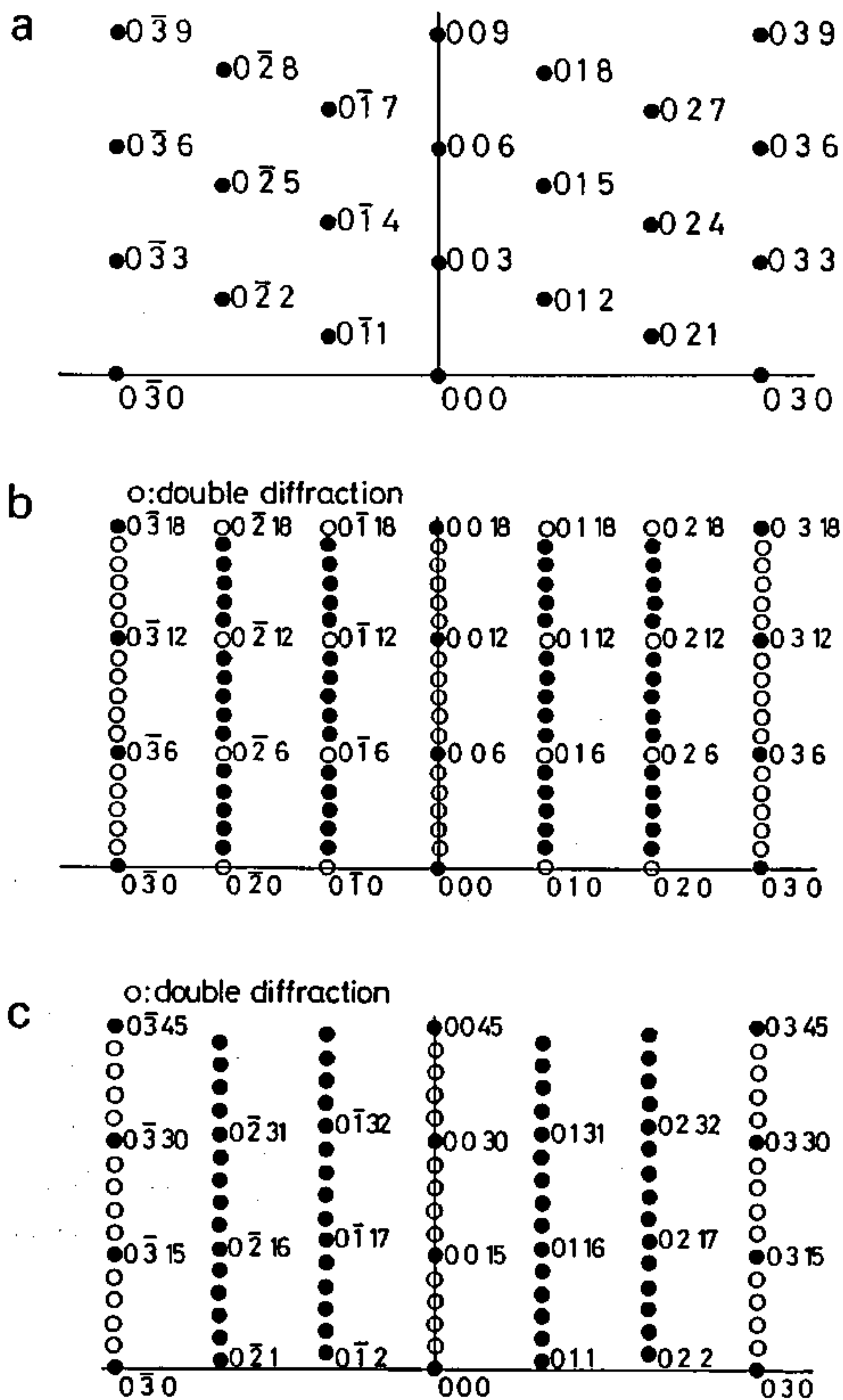


Fig.13 Theoretical <100> azimuth RHEED patterns for (a)3C-, (b)6H- and (c)15R-SiC(0001). Spots represented by white circles appear by double diffraction.

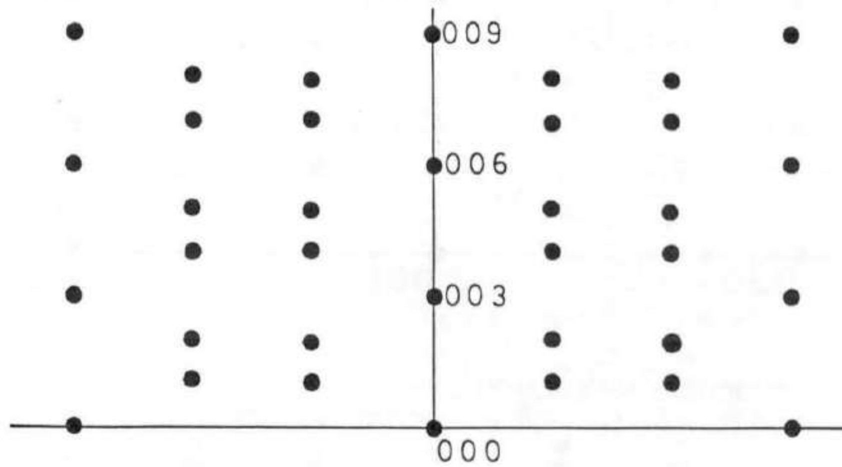


Fig.14 <100> azimuth RHEED pattern of 3C-SiC(0001) containing twining.

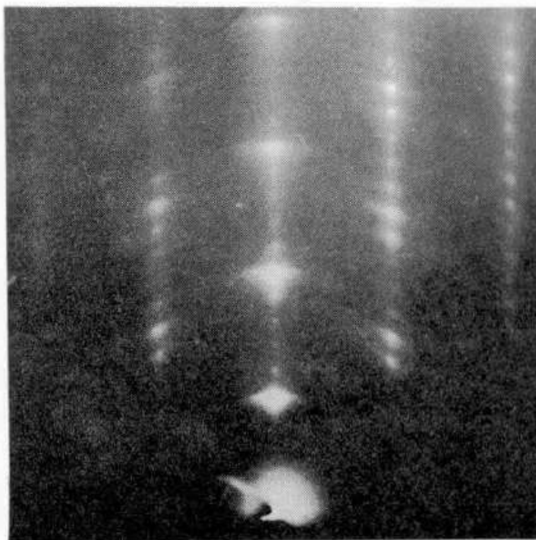


Fig.15 <010> azimuth RHEED pattern of 15R-SiC(0001). Surface of the sample was slightly lapped to obtain a spot pattern.

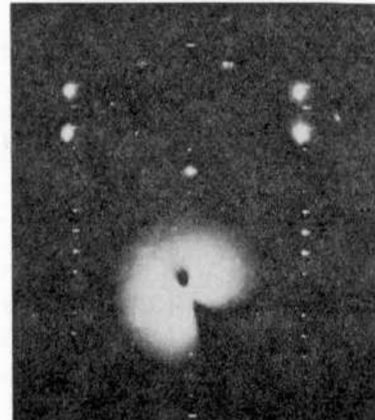


Fig.16 simultaneously obtained a RHEED pattern of a 3C-SiC grown layer and a TED pattern of a 6H-SiC substrate.

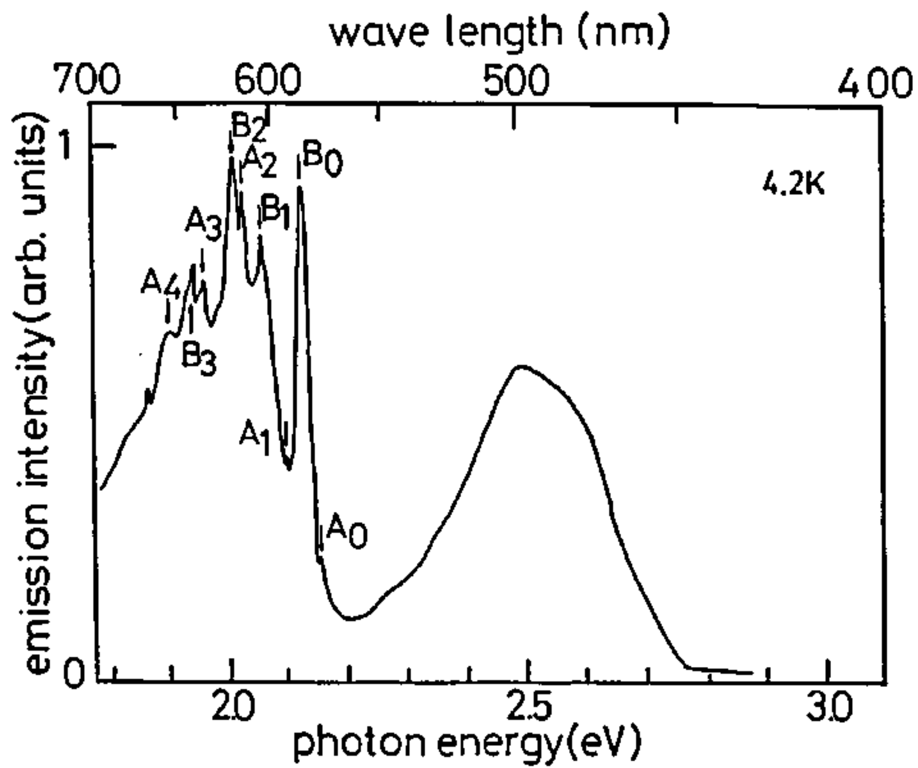


Fig.17 Photoluminescence spectrum of an Al-doped 3C-SiC grown layer. A broad peak at about 2.5eV is due to a 6H-SiC substrate.

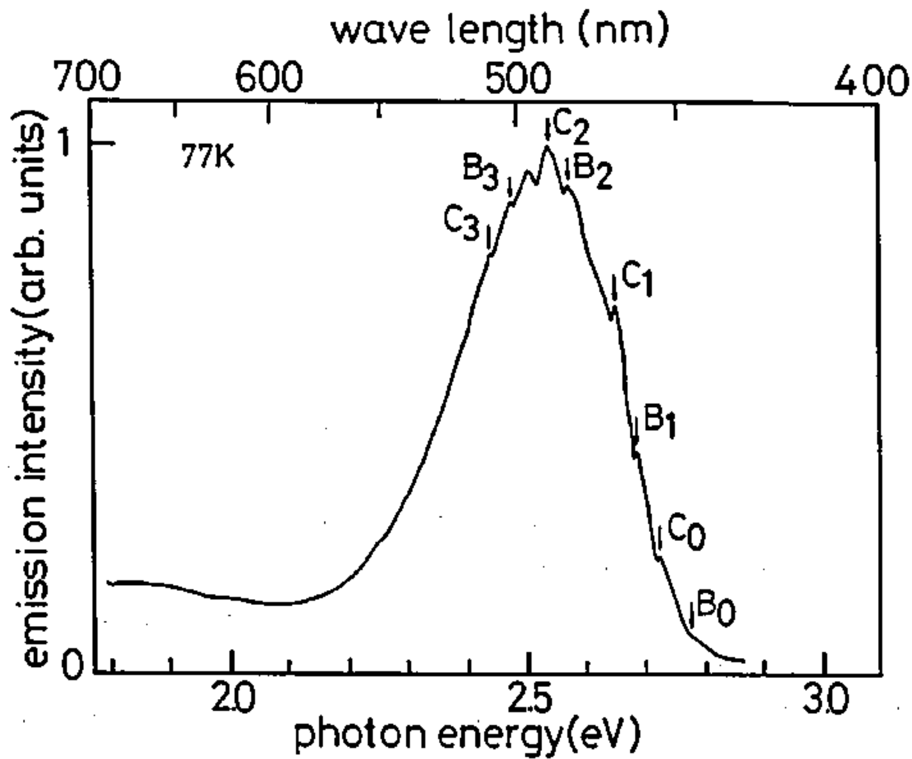


Fig.18 Photoluminescence spectrum of an Al-doped 6H-SiC grown layer.

molten KOH etching was utilized. Before etching, most samples showed streak patterns and identification of polytypes were impossible. After etching, spot patterns were obtained as shown in Figs.4 and 7. By comparing these patterns experimentally obtained with theoretical patterns shown in Figs.13 and 14, the polytypes of the grown layers were clearly identified as concluded in the previous section. When the surface of the grown layer was very rough, a spot pattern was obtained without special treatments as shown in Fig.16. In this figure a RHEED pattern of a grown layer and a TED pattern of a substrate were simultaneously obtained by exposing electron beam to the edge of the sample. Epitaxial growth of 3C-SiC containing twinning on 6H-SiC is clear in this photograph.

(Photoluminescence)

The bandgap energy and the activation energies of impurities are peculiar to each polytype. Therefore, by measuring photoluminescence spectra polytypes can be identified. Since SiC has an indirect band structure and acceptor-related light emission is mainly observed, acceptor doping is desirable to obtain bright luminescence. In this study Al-doping was carried out using TMA and TEA as mentioned in Chapter 4.

Figure 17 shows a photoluminescence spectrum of a grown layer on a natural face. One broad peak at about 2.5eV and a set of peaks under 2.2eV were observed. The broad peak was the luminescence from the substrate and the other peaks are due to the grown layer. The narrow peaks named as A_0 and B_0 were identified as free to bound-acceptor emission and donor-acceptor(N and Al) pair recombination in 3C-SiC, respectively, by comparing with reported spectra[15,18]. A_n and B_n(n is an integer) peaks were phonon replicas of A_0 and B_0, respectively.

Figure 18 shows a photoluminescence spectrum of a grown layer on a lapped face. The peaks under 2.2eV disappeared. The broad peak in Fig.17 at about 2.5eV changed to a set of narrow peaks. These peaks are due to donor-acceptor(N and Al) pair recombination in 6H-SiC. B_n and C_n series were reported to

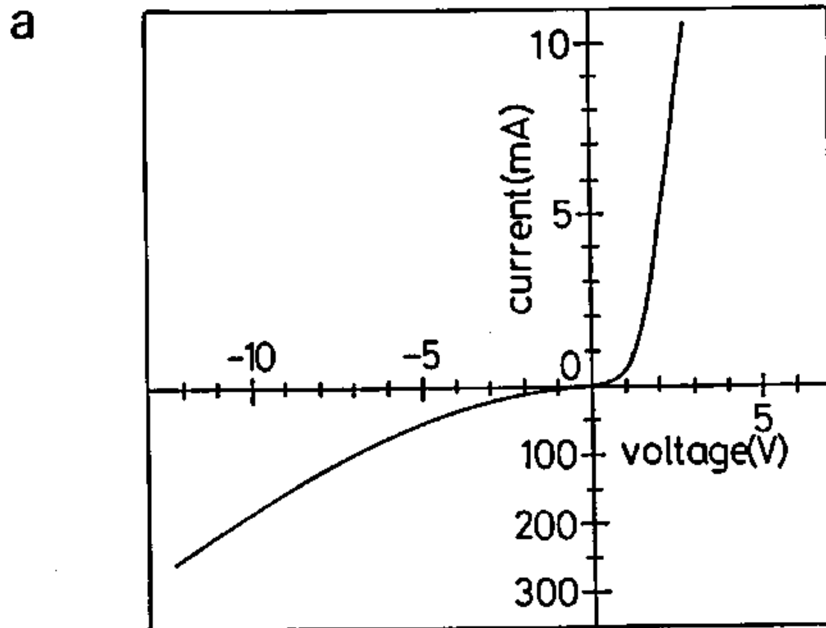
originate from N donors occupying a hexagonallike site and a cubiclike site[19], respectively. In 6H-SiC impurities occupying different sites have different activation energies.

4. Fabrication of Schottky and p-n junction diodes

The growth temperature of 6H-SiC evaluated in this section was 1500°C. Though even at 1400°C 6H-SiC could be grown, the electrical properties of the grown layers were not yet evaluated. Figures 19(a) and (b) show current-voltage characteristics of Au-SiC Schottky diodes on a 6H-SiC grown layer and on a 3C-SiC grown layer containing twinning. Surface treatment before vacuum evaporation of Au was carried out similar to the case of 3C-SiC on Si mentioned in Chapter 4. The conduction type of undoped 6H- and 3C-type grown layers was found to be n-type by a direction of their rectification. Schottky diodes fabricated on 6H-SiC grown layers showed good rectification reproducibly. By C-V characteristics of the diodes undoped donor concentration was obtained as $2 \times 10^{16} cm^{-3}$. Rectification of the diodes on 3C-SiC grown layers was worse than that of 6H-SiC. Twin boundaries in 3C-SiC grown layers were one of the candidates for the origin of the poor rectification.

Utilizing Au-SiC Schottky barriers EBIC observation was carried out. Figures 20(a) and (b) show SEM and EBIC image photographs of 3C-SiC on natural faces. In an EBIC image boundary-like recombination centers are observed. They clearly correspond to twin boundaries observed in the SEM image as grooves. In addition to the twin boundaries recombination centers with equilateral triangular shapes are observed. Probably they are stacking faults. In the EBIC image of the 6H-SiC grown layer recombination centers with a shape of an acute triangle and random lines were observed as shown in Fig.21. Their origin was not clear. Their density widely changed due to observation points in the sample. Used substrates were grown by Acheson method to produce polishing powder and their quality was not uniform.

a



b

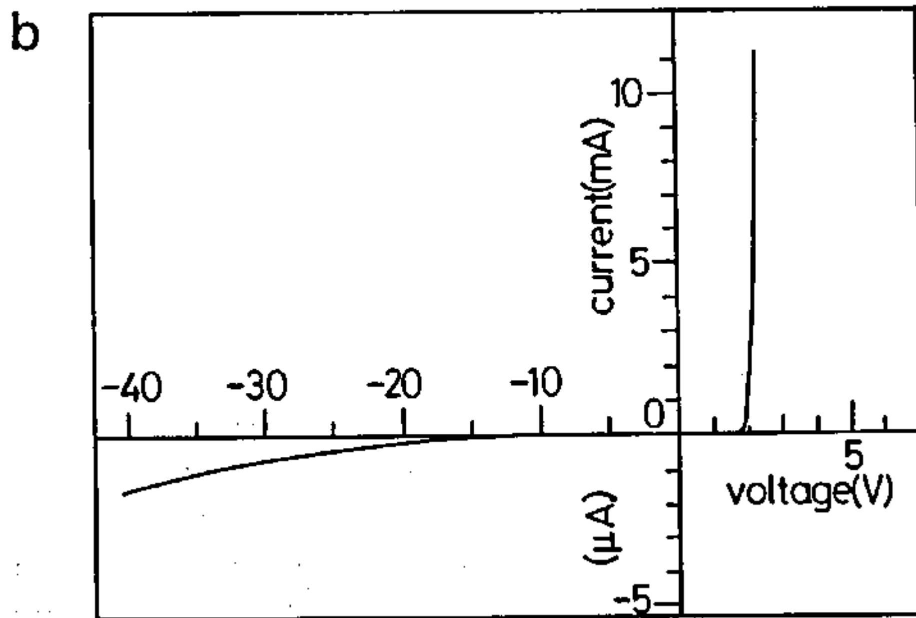


Fig.19 Current-voltage characteristics of a Au-SiC Schottky diodes on (a)6H-SiC and (b)3C-SiC grown layers.

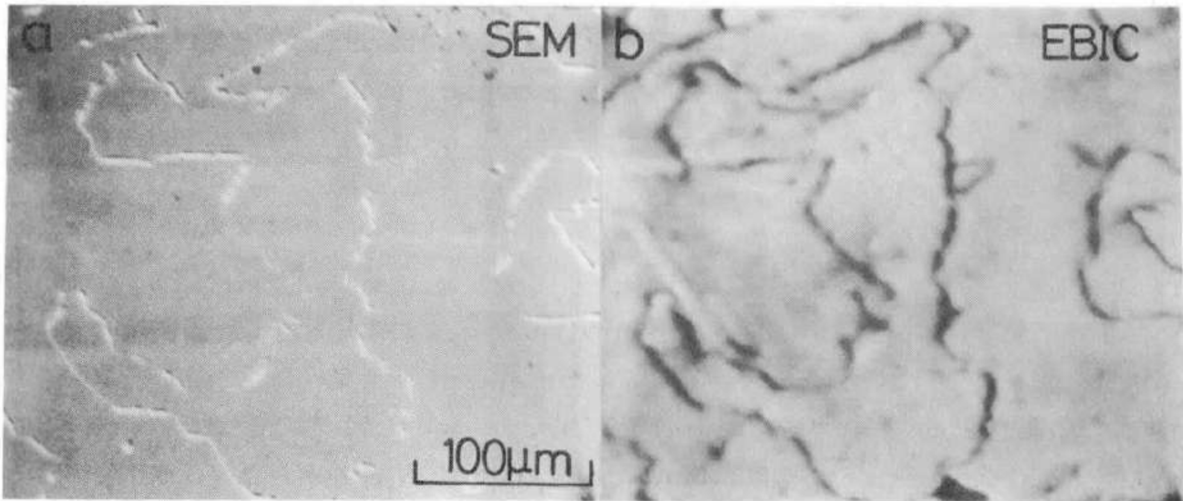


Fig.20 (a)SEM and (b)EBIC images of 3C-SiC grown layers. In EBIC image twin boundaries were observed as recombination centers.

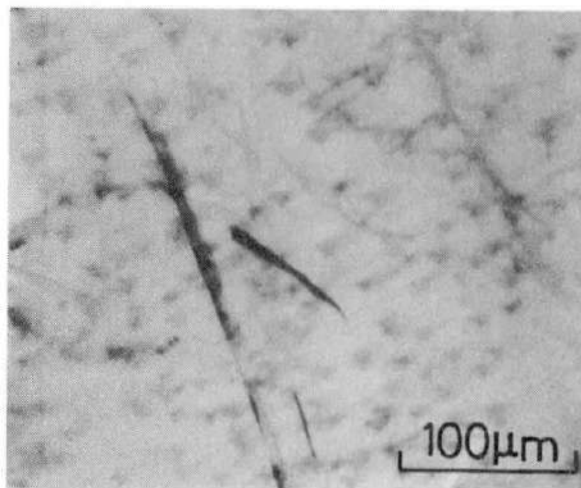


Fig.21 EBIC image of a 6H-SiC grown layer.

Therefore, the grown layers were considered to inherit the quality of the substrates.

Mesa-type p-n junction diodes were fabricated using 6H-SiC on lapped faces. To obtain p-type layers TMA or TEA was introduced by a bubbling method using H_2 during the epitaxial growth. P-type conduction with a carrier density of $4\text{-}9\times10^{17}cm^{-3}$ was confirmed by the van der Pauw method. TMA and TEA work as p-type dopants and carbon sources at the same time. Therefore, the flow rate of C_3H_8 was reduced relatively to that of SiH_4 during the growth of p-type layers. If it was not reduced, the surface of the p-type grown layers became rough. The structure of the fabricated diodes is shown in Fig.22. The undoped n-layer and Al-doped p-layer were grown consecutively. TMA was used for p-type doping. The thickness of both the n- and p-layers was about 2μm. To form mesa structures reactive ion etching(RIE)[20] was utilized with an Al mask using CF_4 and O_2 gases at 10Pa. The junction area of the fabricated diodes was $1.96\times10^{-3}cm^2$. A thermal oxide film of SiO_2 was formed at 1050°C for 6hrs to passivate the surface. Al-Si and Ni were evaporated and alloyed for p-type and n-type ohmic contacts, respectively. Figure 23 shows I-V characteristics of the fabricated p-n junction diode which showed the highest breakdown voltage of 100V. A $1/C^3$-V plotting of capacitance-voltage characteristics showed a proportional relationship(Fig.24), which means that this diode had a graded junction. However, the C-V characteristics of other diodes sometimes indicated abrupt junctions showing a proportional relationship in $1/C^2$-V plottings. The scattered C-V characteristics are probably attributed to gas-flow switching to start the growth of p-SiC on n-SiC.

Breakdown electric field was calculated using the I-V and $1/C^3$-V characteristics shown in Figs.23 and 24, respectively. Breakdown voltage(V_b) and the maximum electric field(E_m) in a graded p-n junction have the following relationship[21]

$$V_b=(4/3)E_m^{3/2}(2\varepsilon_s/aq)^{(1/2)} , \qquad (1)$$

where a is impurity gradient(cm^{-4}), ε_s semiconductor permittivity and q elementary charge. The impurity gradient can be obtained

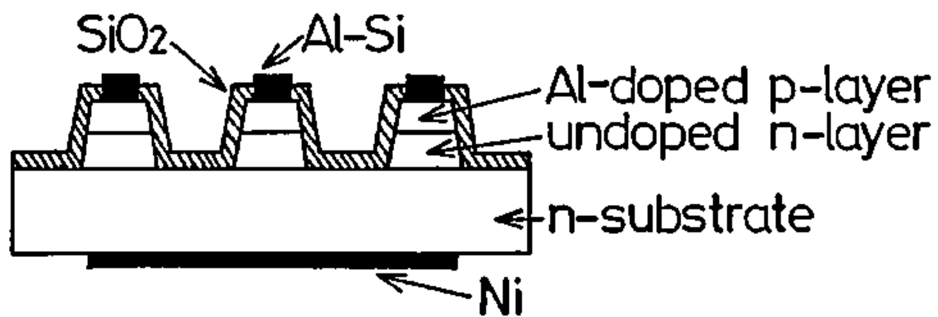


Fig.22 Schematic cross section of p-n junction mesa-diodes fabricated using 6H-SiC grown layers.

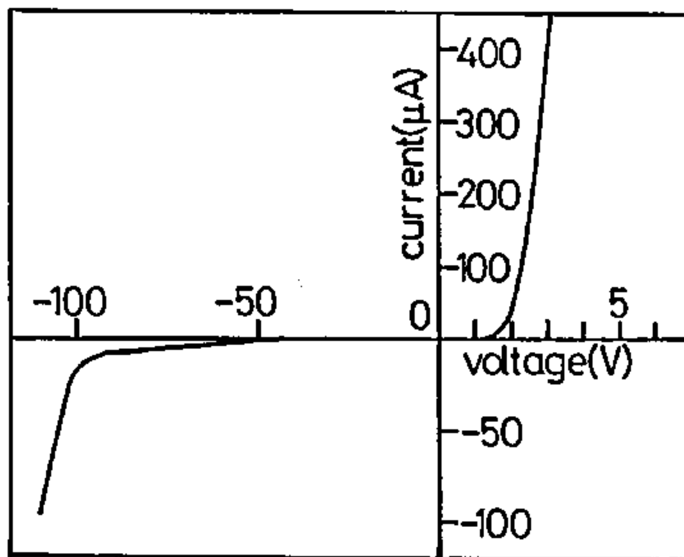


Fig.23 Current-voltage characteristics of a fabricated p-n junction diode.

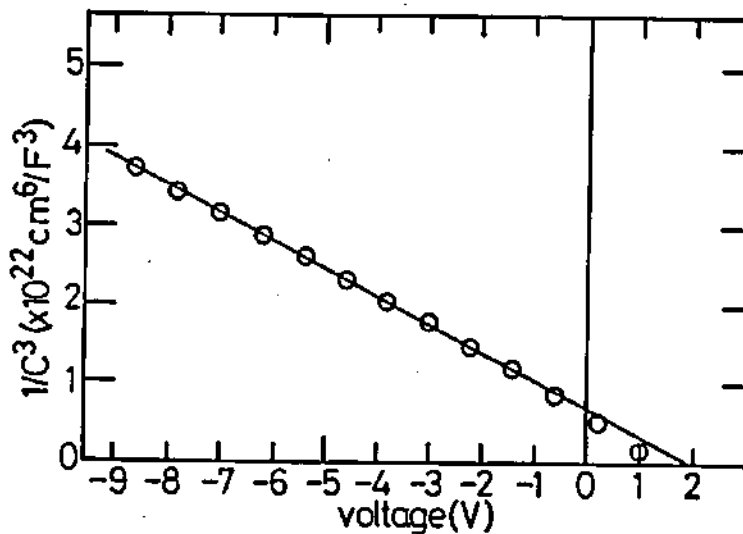


Fig.24 $1/C^3$-V plotting of capacitance-voltage characteristics of the p-n junction diode.

from the slope of the $1/C^3$-V plotting utilizing the next formula[21]

$$1/C^3=12(V_{bi}-V)/(qa\varepsilon_s^2) , \qquad (2)$$

where V_{bi} is built-in potential, C depletion-layer capacitance and V applied voltage. Thus the breakdown electric field was estimated to be 2.4×10^6 V/cm. von Muench et al. fabricated a onesided abrupt p-n$^+$ junction diode at 1800°C by CVD method and they obtained a breakdown electric field of 2-3.7×10^6 V/cm[22]. They compared the results with an empirical prediction by Sze and Gibbsons[23] mentioned in Chapter 4 and concluded that the experimentally obtained value of V_B(breakdown voltage) and E_m(maximum field in a junction) were larger than the prediction and the prediction cannot be applied to SiC. For graded junctions Sze and Gibbsons gave the following relationship between V_B and a[23].

$$V_B=60(E_g/1.1)^{6/5}(a/3\times10^{20})^{-2/5} \quad (V) , \qquad (3)$$

where E_g is bandgap energy. The relationship between V_B and E_m is given as eq.(1). Figures 25(a) and (b) show V_B and E_m as a function of a. Experimentally obtained V_B and E_m are plotted as circles in the figures and they are obviously larger than Sze and Gibbsons' prediction. Conclusively, in this work of preliminary trials utilizing low-temperature growth, comparable results to high-temperature grown layers were obtained.

These p-n junction diodes showed blue light-emission in the forward-biased region. Examples of electroluminescence spectra are shown in Fig.26. The diodes were driven by a pulse current of 500Hz with a duty cycle of 0.4. The wavelengths of the peaks in the spectra well agreed with those of LED's grown by liquid phase epitaxy(LPE)[24]. The peaks are attributed to three origins. The highest-energy peak at 425nm(F peak) and the peak at 455nm(E peak) are considered to be due to free-exciton recombination and Al-related localized centers, respectively. The other peaks(M peaks) are concerned with donor-acceptor(N and Al) pair recombinations.

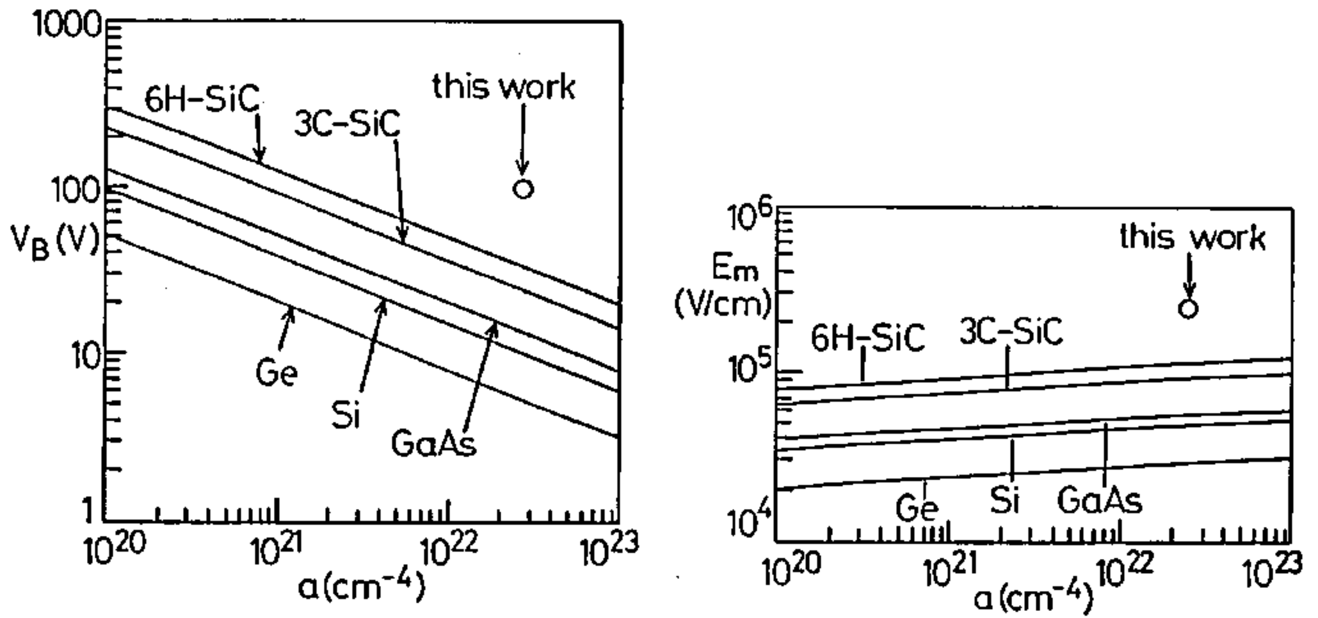


Fig.25 Predicted (a)V_B(breakdown voltage) and (b)E_m(maximum field) for graded p-n junction as a function of a(impurity gradient). Used formulas were given by Sze and Gibbsons[23]. A white circles represent results of this investigation.

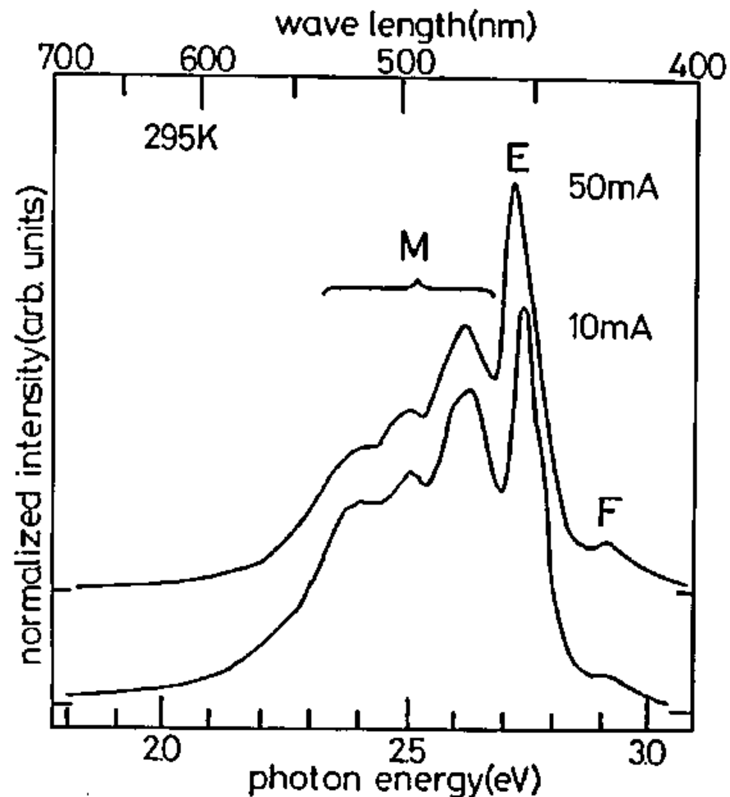


Fig.26 Electroluminescence spectra of a fabricated p-n junction diode at room temperature.

5. Summary

SiC was grown on 6H-SiC(0001)Si faces at 1350-1500°C by CVD method. Polytypes of grown layers were changed by changing growth temperatures and the orientation of substrates. In this temperature region, 3C-SiC containing twinning was obtained on a natural face. However, 6H-SiC was grown on off oriented (0001) substrates at 1400-1500°C. This temperature is 300-400°C lower than necessary growth temperature for 6H-SiC. The change in polytypes by off orientation of substrates was explained in relation to the surface step density. Polytypes of the grown layers were identified utilizing etch pits, RHEED patterns and PL spectra.

P-n junction diodes fabricated using the 6H-SiC grown layers showed good rectification. A breakdown electric field of 2.4×10^{6}V/cm was achieved in the p-n junction. This fact indicates that the crystallinity of 6H-SiC grown at low temperatures by introduction of off-orientation is comparable to that of grown at high temperatures.

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