

V. ION IMPLANTATION INTO 3C-SiC GROWN LAYERS AND APPLICATION TO MOSFET'S

1. Introduction

A selective doping technique is indispensable in fabrication of electronic devices especially for IC(integrated circuits). There are two major techniques for selective doping, namely, diffusion and ion implantation methods. Both methods are popular for a Si process. However, in the case of SiC the diffusion method is hard to apply, because the diffusion coefficients of impurities in SiC are very low. Campbell and Chang fabricated junction-gate FET's of α -SiC using a diffusion technique[1]. They reported that diffusion of Al into α -SiC required temperatures from 1800°C to 2100°C. Moreover, a special masking technique utilizing SiC was necessary. Thus, the diffusion method seems to be not practical for SiC. Ion implantation into α -SiC was attempted by many investigators[2-6]. Marsh investigated the activation of implanted impurities using various dopants[2]. Though the implantation of donor impurities such as N, P, Sb and Bi was successful, samples implanted with acceptors were high resistive even after annealing and the acceptors could not be activated. They explained that deep donor-type defects induced by the implantation prevented the activation of the implanted acceptors. Concerning 3C-SiC Kalinina et al.[7] reported a successful fabrication of p-n junction diodes by implantation of Al, however, they did not describe details of investigation. Though Kondo et al.[8] attempted hot implantation(specimens were intentionally heated during implantation) in addition to the standard implantation, the activation was unsuccessful. Edmond et al.[9] reported successful fabrication of p-n junction diodes by hot implantation of Al into undoped layers without annealing. The crystal growth methods of these two groups are similar to that of this investigation. The difference in their investigations is not clear.

In this investigation, implantation of N_2^+ and P^+ was attempted. The electrical characteristics of implanted layers were evaluated changing annealing temperatures. Planar-type p-n junction diodes were fabricated using the implantation technique.

The first successful fabrication of n-channel inversion-type MOSFET's is mentioned. The MOSFET's were fabricated by the combination of ion implantation and thermal oxidation techniques which are ordinary in the Si process.

2. Activation of implanted donors

Ion implantation of N_2^+ and P^+ was carried out into B-doped grown layers. High resistive ($\rho \geq 200 \Omega \text{cm}$) B-doped layers were suitable for characterization of thin n^+ layers formed by implantation of donors. The thickness of the B-doped grown layers was about $6 \mu\text{m}$. APD-free grown layers on 2° off substrates were used. Samples were tilted at 7° during the implantation to avoid a channeling effect. The current density of an ion beam was lower than $0.25 \mu\text{A}/\text{cm}^2$. Therefore, heating by the beam during the implantation was negligible[10].

The conditions of the ion implantation were listed in Table 1. The implantation was carried out by successive two steps to improve the uniformity of implanted impurities. The first implantation was high dose with high energy and the second was low dose with low energy. Figure 1 shows a calculated profile of implanted P using the projected average range and projected standard deviation in the literatures[11-13] for a total dose of $1.3 \times 10^{15} \text{cm}^{-2}$ (condition 1 in Table 1). In the case of condition 2, the total dose was decreased to 30% of that in condition 1 with the same energy. N_2^+ implantation with a total dose of $1.95 \times 10^{14} \text{cm}^{-2}$ (condition 3) corresponds to N^+ implantation with a dose of $3.9 \times 10^{14} \text{cm}^{-2}$ which is the same dose level as condition 2. The energy of the N_2^+ implantation was decided to have the nearly same impurity profile[13] as in P^+ implantation of condition 2. After the implantation samples were annealed in

No.	implanted ion	1st dose(cm^{-2}) 2nd	1st energy(eV) 2nd	total dose (cm^{-2})
1	P^+	1×10^{15} 3×10^{14}	100K 25K	1.3×10^{15}
2	P^+	3×10^{14} 9×10^{13}	100K 25K	3.9×10^{14}
3	N_2^+	1.5×10^{14} 4.5×10^{13}	100K 25K	1.95×10^{14}

Table 1 Conditions of ion implantation.

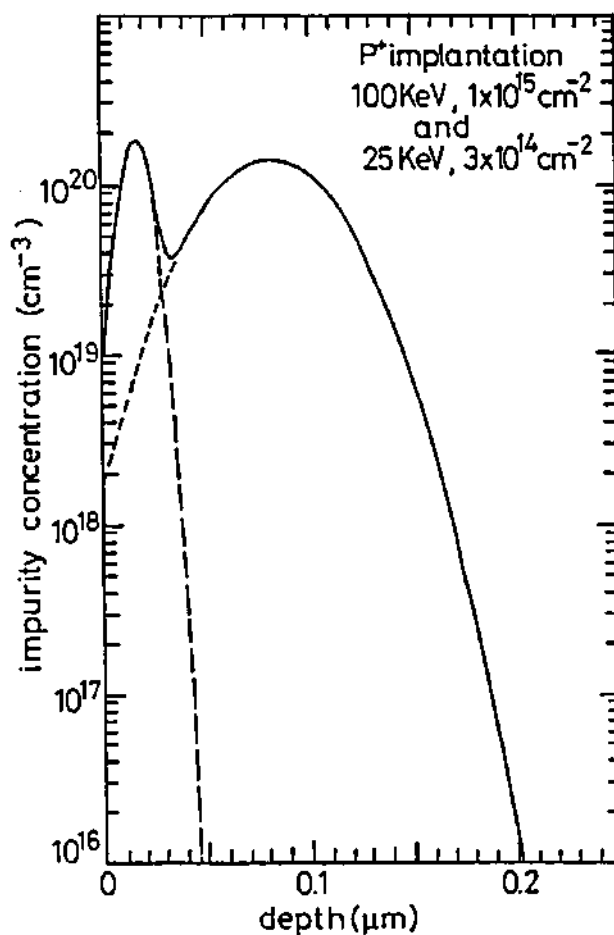


Fig.1 Calculated profile of implanted P with a total dose of $1.3 \times 10^{15} \text{ cm}^{-2}$. Details of conditions of implantaion are listed in Table 1.

Ar atmosphere for 30min. The samples were heated by RF inductive heating. By SIMS analysis the annealed specimen showed almost the same depth profile of implanted P as that without annealing by SIMS analysis.

Figure 2(a) shows a RHEED halo pattern of an as-implanted sample. The ion implantation was carried out under condition 1(P⁺, total dose: $1.3 \times 10^{15} \text{cm}^{-2}$). The halo pattern indicates that the implanted layer was amorphous. Figure 2(b) shows a RHEED pattern of the sample after annealing at 800°C. Recrystallization to a single crystal was clearly observed. Annealing temperature was changed up to 1300°C. However, no significant difference in RHEED patterns compared with Fig.2(b) was observed. Samples implanted under condition 2(P⁺, total dose: $3.9 \times 10^{14} \text{cm}^{-2}$) showed similar results. The implanted samples could be told from not implanted samples with naked eyes by noticing a slight difference in colors. The refractive index of the implanted layers changed by amorphization and interference took place. The difference in colors vanished by annealing.

Sheet resistance of the implanted layers was evaluated by the four-point probe method or by van der Pauw method. Si substrates of the specimens for van der Pauw measurement were removed by a mixed solution of HNO₃ and HF before the measurement to avoid errors due to current conduction through the substrates. N-type conduction was confirmed for both the P⁺ and N₂⁺ implanted layers by van der Pauw method. As shown in Fig.3, the sheet resistance monotonously decreased as annealing temperature increased and it reached to about $10^3 \Omega/\square$ by annealing at about 1350°C.

Electrical activation rates were estimated by van der Pauw measurement. The electrical activation rate was defined as the ratio of sheet carrier concentration and total dose. The electrical activation rates were improved by raising annealing temperatures as shown in Fig.4. The P⁺ implanted layer with a total dose of $3.9 \times 10^{14} \text{cm}^{-2}$ (condition 2) gave the higher electrical activation rates than those for a total dose of $1.3 \times 10^{15} \text{cm}^{-2}$ (condition 1). The N₂⁺ implanted layers gave the

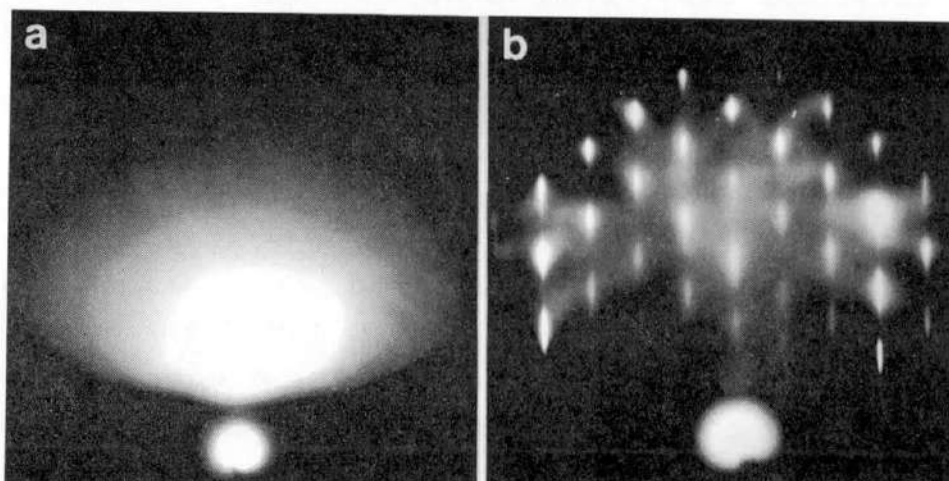


Fig.2 RHEED patterns of P^+ implanted layers. (a)Before and (b)after annealing at 800°C .

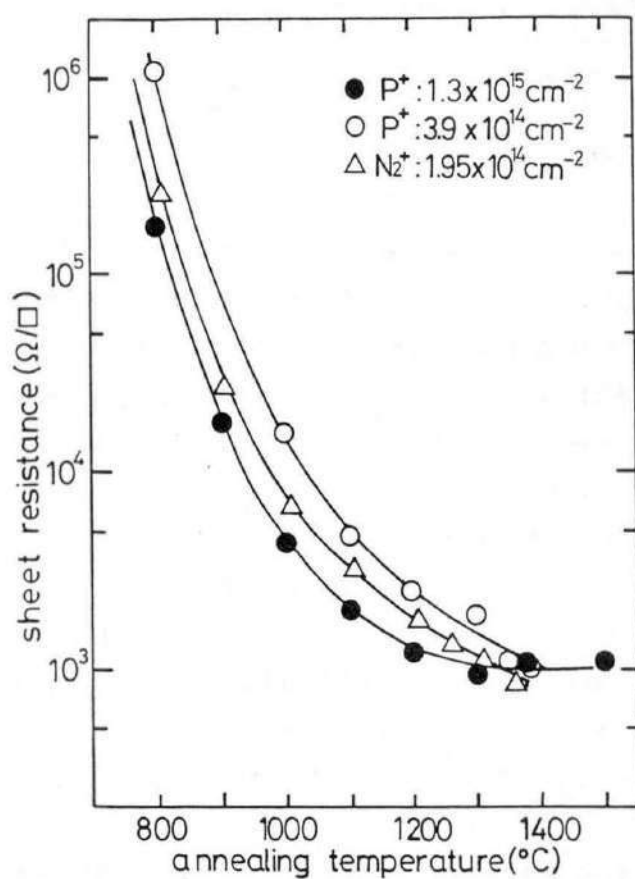


Fig.3 Sheet resistance of implanted layers as a function of annealing temperatures.

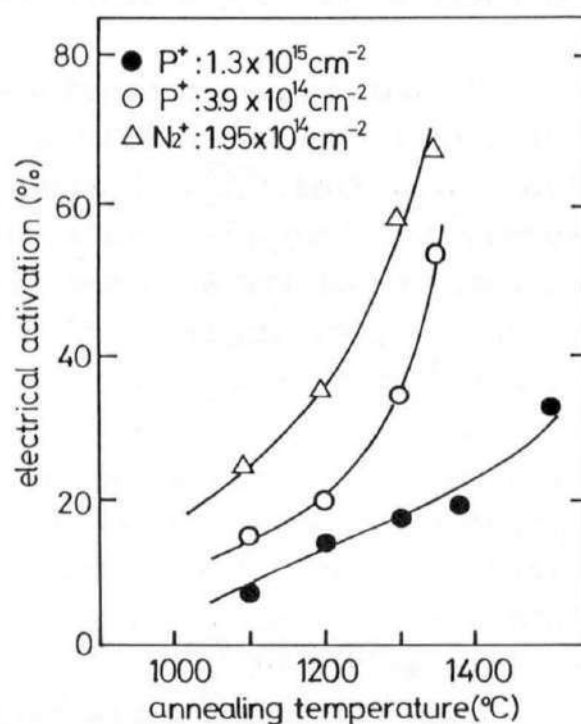


Fig.4 Electrical activation rate as a function of annealing temperatures.

higher electrical activation rates than the P^+ implanted layers, which is similar to implantation into 6H-SiC[2]. Bridge-type specimens were fabricated by the P^+ implantation to carry out the standard Hall measurement and to investigate electrical anisotropy in the implanted layers. Such specimens were fabricated by a selective implantation utilizing a deposited SiO_2 film as a mask. The implantation was carried out under condition 2. Concerning conditions 1 and 3 the standard Hall measurement was not carried out yet. The electrical activation rates obtained by the standard Hall measurement well agreed with those obtained by van der Pauw measurement. The electron mobility obtained by van der Pauw method was about $30\text{cm}^2/\text{Vs}$ in all cases. The electron mobility obtained by the standard Hall measurement showed electrical anisotropy similar to the undoped grown layers. $\mu_{||}$ and $\mu_{\perp}$ were about 50 and $25\text{cm}^2/\text{Vs}$, respectively.

3. Fabrication of p-n junction diode

Planar-type p-n junction diodes were fabricated using the ion implantation technique. Figure 5 shows the structure of fabricated diodes. An Al-doped p-layer was grown on a 2° off p-Si substrate. Typical hole concentration, hole mobility and resistivity of the Al-doped layer were $3.5 \times 10^{17}\text{cm}^{-3}$, $32\text{cm}^2/\text{Vs}$ and $0.56\Omega\text{cm}$, respectively. P^+ implantation with a total dose of $3.9 \times 10^{14}\text{cm}^{-2}$ or N_2^+ with a total dose of $1.95 \times 10^{14}\text{cm}^{-2}$ was carried out to obtain n-layers. Deposited SiO_2 of 500nm in thickness was used as a mask for the implantation. Annealing temperatures were 1100°C , 1200°C and 1300°C . Annealing time was fixed at 30 min. Finally ohmic contacts were formed using Al and AuGa for n-SiC and p-Si, respectively. The area of the fabricated diodes was $7.1 \times 10^{-4}\text{cm}^2$.

Current-voltage characteristics of the P^+ and N_2^+ implanted diodes were shown in Figs.6(a) and (b), respectively. Both the P^+ and N_2^+ implanted diodes showed similar results. Rectification of the diodes annealed at 1100°C and 1200°C was superior to those

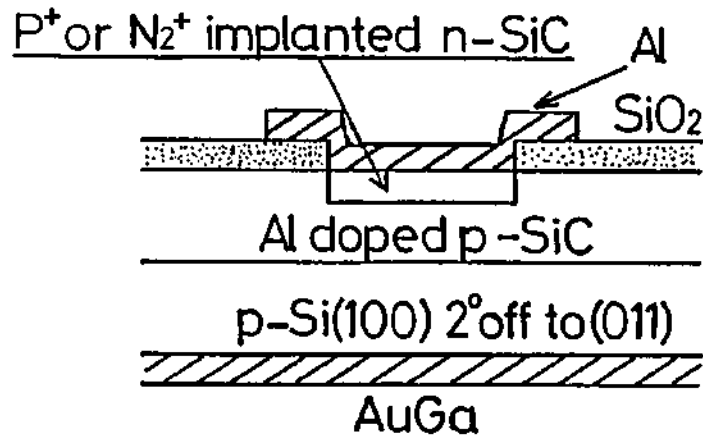


Fig.5 Schematic cross section of planar type p-n junction diodes fabricated by the ion implantation.

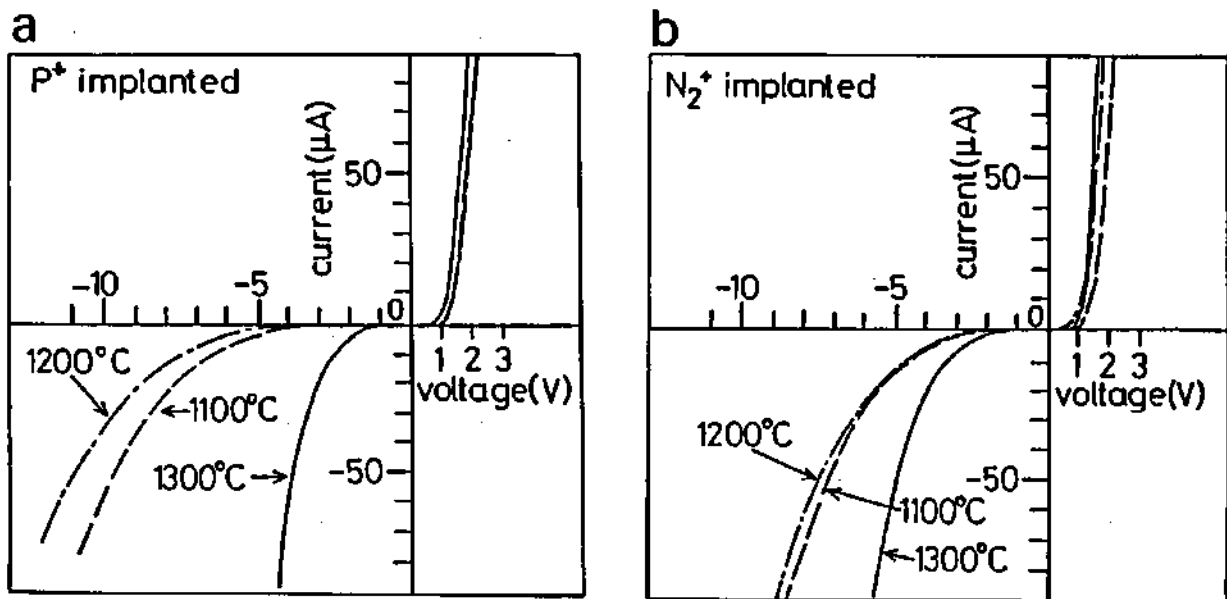


Fig.6 Current-voltage characteristics of p-n junction diodes fabricated by (a)P⁺ and (b)N₂⁺ implantation.

at 1300°C. As shown in Fig.4, the electrical activation rate increased abruptly by annealing at temperatures over 1300°C. And so, this annealing temperature dependence of the rectification was considered to be related to the change from an n-layer to an n⁺-layer because of increase in the electrical activation rate. The best ideal diode factor of 3.8 was obtained when annealing temperature was 1100°C for both the P⁺ and N₂⁺ implanted diodes.

Capacitance-voltage characteristics of these diodes showed small variation in capacitance as shown in Fig.7. As annealing temperatures were raised, the capacitance and the magnitude of its variation became larger. These results mean that the diodes had p-i-n structures[14] and the thickness of the i layer became thinner as annealing temperature became higher. The N₂⁺ implanted diodes showed the larger capacitance and its variation than the P⁺ implanted diodes. This difference was considered to originate from the difference in electrical activation. The N₂⁺ implanted layers showed the higher electrical activation rates than the P⁺ implanted layers as mentioned in the previous section. Hence, the thicknesses of the i layers were thinner in the N₂⁺ implanted diodes and the capacitance became larger.

4. Fabrication of MOSFET's

MOSFET's were fabricated using the ion implantation technique. A schematic cross section of the fabricated MOSFET's is shown in Fig.8. A channel layer of B-doped p-SiC with the thickness of 2μm was grown on undoped n-SiC with the thickness of 7μm. Since there is large lattice mismatch between Si and SiC, the layer with the thickness of over several microns was necessary to reduce crystal defects and to improve device characteristics by our present technique. Source and drain were formed by the ion implantation of P⁺ using deposited SiO₂ with the thickness of 500nm as a mask. The implantation was carried out under the condition 1 in Table 1. Annealing after the implantation was carried out in an IR radiative heating furnace

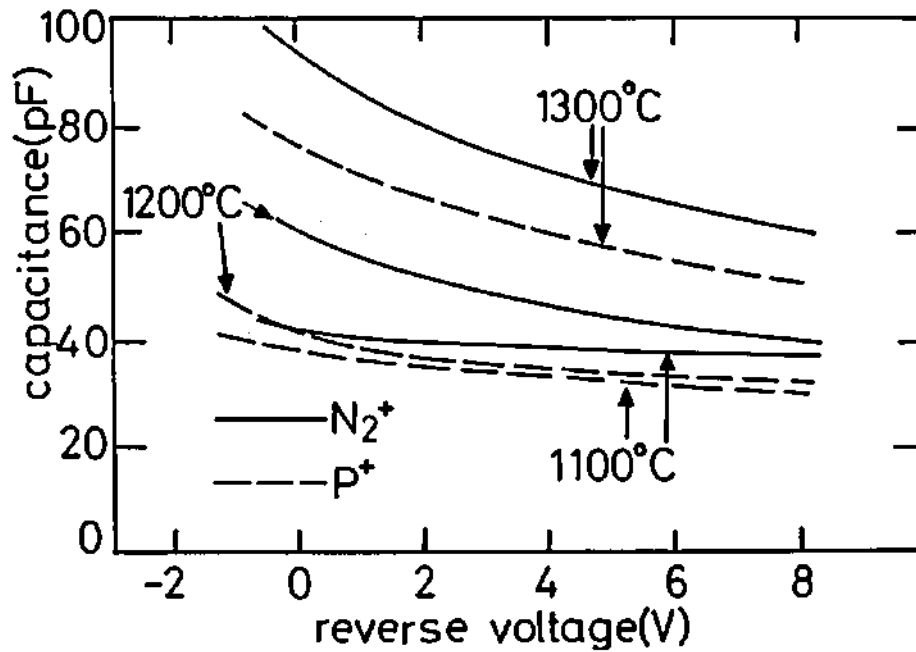


Fig.7 Capacitance-voltage characteristics of p-n junction diodes.

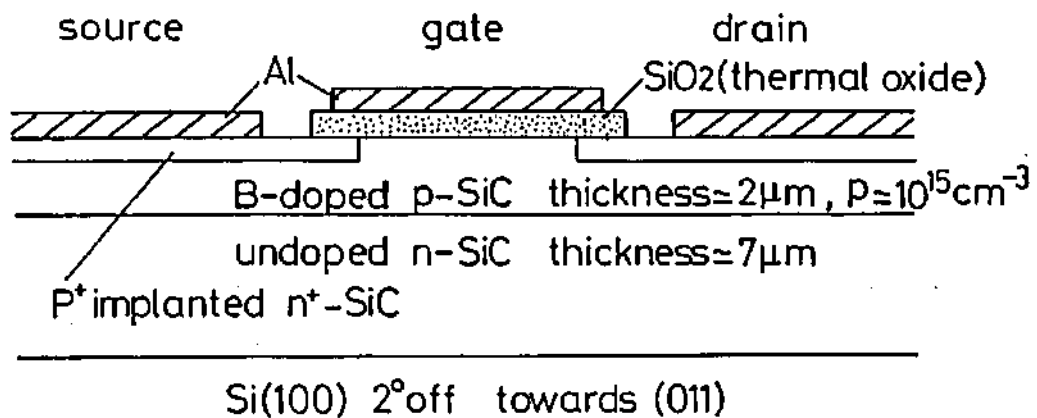


Fig.8 Schematic cross section of fabricated MOSFET's.

in Ar atmosphere at 1080°C for 1hr.

A gate insulator was formed by thermal oxidation of SiC at 1050°C using dry oxygen for 6hrs. The thermal oxide film of 3C-SiC was found to be SiO₂ and inversion was confirmed under an illuminated condition in an Al/SiO₂/n-SiC structure[15]. Typical electrical resistivity and breakdown electric field of SiO₂ formed by the thermal oxidation were $8.5 \times 10^{15} \Omega \text{cm}$ and $2.5 \times 10^6 \text{V/cm}$, respectively. The thickness of the gate oxide was about 60nm. The gate length and the width are 20 μm and 500 μm , respectively. Al was used as a gate electrode and ohmic contacts for source and drain. Alloying of the ohmic contacts was not carried out. The top view of the fabricated MOSFET is shown in Fig.9.

Current-voltage characteristics of the FET at 310K are shown in Fig.10. The sample was not illuminated. An action of inversion-type MOSFET's was achieved for the first time. Kinks in the saturation region were observed. Such kinks are known as a feature of SOI(Si-on-insulator) MOSFET's[16,17]. Since in this investigation the MOSFET's were fabricated on a high resistive B-doped p-layer, their characteristics were considered to show SOI-like features. In Al-SiO₂-SiC MOS diodes, the inversion condition was observed only under illumination, which is due to very low intrinsic carrier concentration($\approx 10 \text{cm}^{-3}$ at 300K) of 3C-SiC[15]. However, the MOSFET's operated without illumination. Electrons which are necessary to form an inversion layer were considered to be supplied from source.

Effective mobility of the FET was estimated using the characteristics in the linear region where drain voltage was lower than the voltage at the beginning of the kink. Ideal characteristics of MOSFET's in the linear region are given by

$$I_d = (W/L) \mu_n C_0 ((V_g - V_{th}) V_d - V_d^2 / 2) , \quad (1)$$

where I_d is drain current, W gate width, L gate length, μ_n electron mobility, V_g gate voltage, V_{th} threshold voltage and V_d drain voltage. Here W/L is 25 and the value of $5.75 \times 10^{-8} \text{F/cm}^2$ was used for C_0 based on an investigation of Al-SiO₂-SiC system[15]. μ_n and $(V_g - V_{th})$ were changed to agree with measured $I_d - V_d$

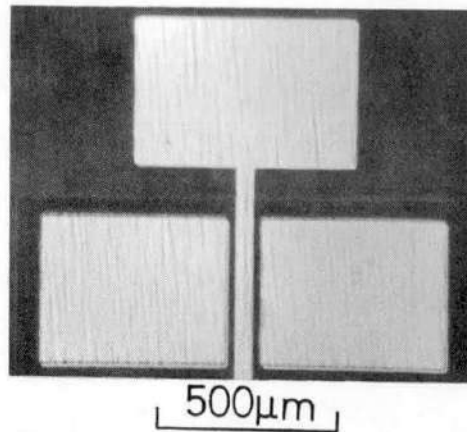


Fig. 9 Top view of a fabricated MOSFET.

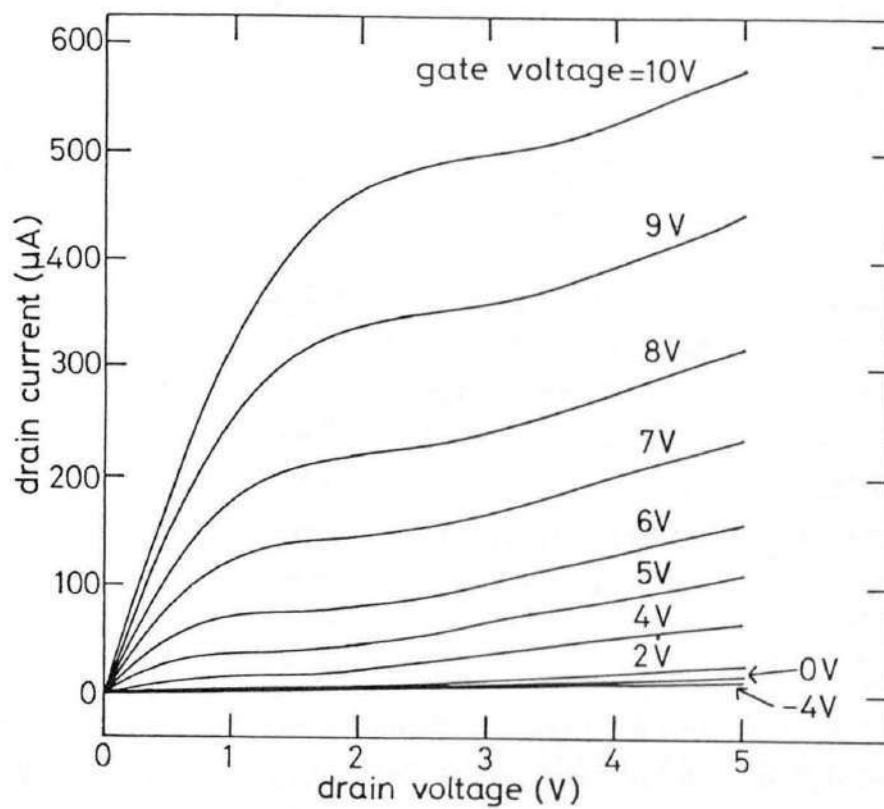


Fig. 10 Current-voltage characteristics of the MOSFET at 310K.

characteristics. The obtained effective electron mobility was about $100\text{cm}^2/\text{Vsec}$.

The measurement of I_d-V_d characteristics at high temperatures was attempted. The MOSFET whose characteristics are shown in Fig.10 did not operate at temperatures above 70°C because of breakdown of gate oxide. Simultaneously fabricated MOSFET's also showed the breakdown of the gate oxide by heating up to 100°C . Such breakdown phenomena are probably attributed to contamination during fabrication. Some other MOSFET's showed variation of I_d as a function of V_g up to 440°C . However, the gate oxide became leaky after heating up to 165°C and it did not recover after cooling. The observed worsening of gate insulation was considered to be attributed to a reaction of Al and SiO_2 . Au gate is effective to prevent such a problem[18]. To realize practical high temperature devices of 3C-SiC a combination of peripheral materials will be an important problem.

5. Summary

Ion implantation of P^+ and N_2^+ into p-type 3C-SiC was carried out. The annealing temperature dependence of electrical properties of implanted layers was investigated up to 1400°C . Electrical activation rates of implanted impurities were improved as annealing temperature became higher. N_2^+ implanted layers showed the larger electrical activation rate than P^+ implanted layers. P-n junction diodes were fabricated using an ion implantation technique. Their capacitance-voltage characteristics indicated that they had a p-i-n structure.

Inversion-type MOSFET's of 3C-SiC were fabricated. Source and drain were formed by the ion implantation of P^+ . Inversion mode operation was confirmed for the first time. Current-voltage characteristics showed kinks in the saturation region which are known as a feature of SOI MOSFET's. Effective electron mobility in the MOSFET's was estimated to be about $100\text{cm}^2/\text{Vs}$. This successful fabrication of MOSFET's showed usefulness of the ion

implantation technique for device fabrication of 3C-SiC.

References

- [1] R.B.Campbel and H.C.Chang, *Semiconductors and Semimetals* Vol.7 Part B, (Academic Press, New York, 1971) edited by R.K.Willardson and A.C.Beer, Chapter 9.
- [2] O.J.Marsh, *Silicon Carbide-1973*, (University of South Carolina Press, Columbia, 1974) edited by R.C.Marshall, J.W.Faust, Jr. and C.E.Ryan., p.471.
- [3] H.L.Dunlap and O.J.Marsh, *Appl. Phys. Lett.* 15(1969) 311.
- [4] A.Addamiano, G.W.Anderson, J.Comas, H.L.Hughes and W.Lucke, *J. Electrochem. Soc.* 119(1972) 1355.
- [5] V.M.Gusev, K.D.Demakov, M.G.Kosaganova, M.B.Reifman and V.G.Stolyarova, *Sov. Phys. Semicond.* 9(1976) 820.
- [6] S.A.Belova, A.V.Vorob'ev, V.M.Gusev, K.D.Demakov, M.G.Kosaganova, N.K.Prokof'eva, M.B.Reifman, V.G.Stolyarova and V.A.Uzhegova, *Sov. Phys. Semicond.* 10(1976) 743.
- [7] E.V.Kalinina, N.K.Prokof'eva, A.V.Suvorov, G.F.Kholuyanov and V.E.Chelnokov, *Sov. Phys. Semicond.* 12(1978) 1372.
- [8] Y.Kondo, T.Takahashi, E.Sakuma and S.Misawa and H.Daimon, S.Yoshida and Y.Hayashi, *Extended Abstr. of the 46th Autumn Meeting of the Japan Society of Applied Physics*, Kyoto, October, 1985, 2p-C-11.
- [9] H.Kong, H.J.Kim, J.A.Edmond, J.W.Palmour, J.Ryu, C.H.Carter, Jr., J.T.Glass and R.F.Davis, *Material Society Symposia Proceedings vol.97*, Anaheim, 1987(Material Research Society, Pittsburgh, 1987) p.232.
- [10] H.Ryssel and I.Ruge, *Ion Implantation*, (John Wiley & Sons, Chichester, 1986), p.116.
- [11] H.Ishiwara and S.Furukawa, *Trans. IECE Japan* 56-C(1973) 179, in Japanese.
- [12] S.Furukawa, H.Matsumura and H.Ishiwara, *Jpn. J. Appl. Phys.* 11(1972) 134.
- [13] J.E.Gibbons, W.S.Johnson and S.W.Mylroie, *Projected Range*

- Statics*, (Halsted Press, Stroudsburg, 1975) 2nd ed.
- [14] H.Matsunami, *Handoutai-kougaku*(Semiconductor Engineering), (Syokoudou, Tokyo, 1983) p.139, in Japanese.
- [15] K.Shibahara, S.Nishino and H.Matsunami, Jpn. J. Appl. Phys. 23(1984) L862.
- [16] J.Tihanyi and H.Schleotterer, Solid-State Electron. 18(1975) 309.
- [17] S.M.Sze, *Physics of Semiconductor Devices*, (John Wiley & Sons, New York, 1981) 2nd edition, Chapter 8.
- [18] E.Sakuma, H.Daimon, M.Yamanaka, S.Misawa, K.Endo and S.Yoshida, Extended Abstr. of the 34th spring Meeting of the Japan Society of Applied Physics and of the related societies, Tokyo, March, 1987, 28p-W-9 and 28p-W-10.